

VHDL Generation

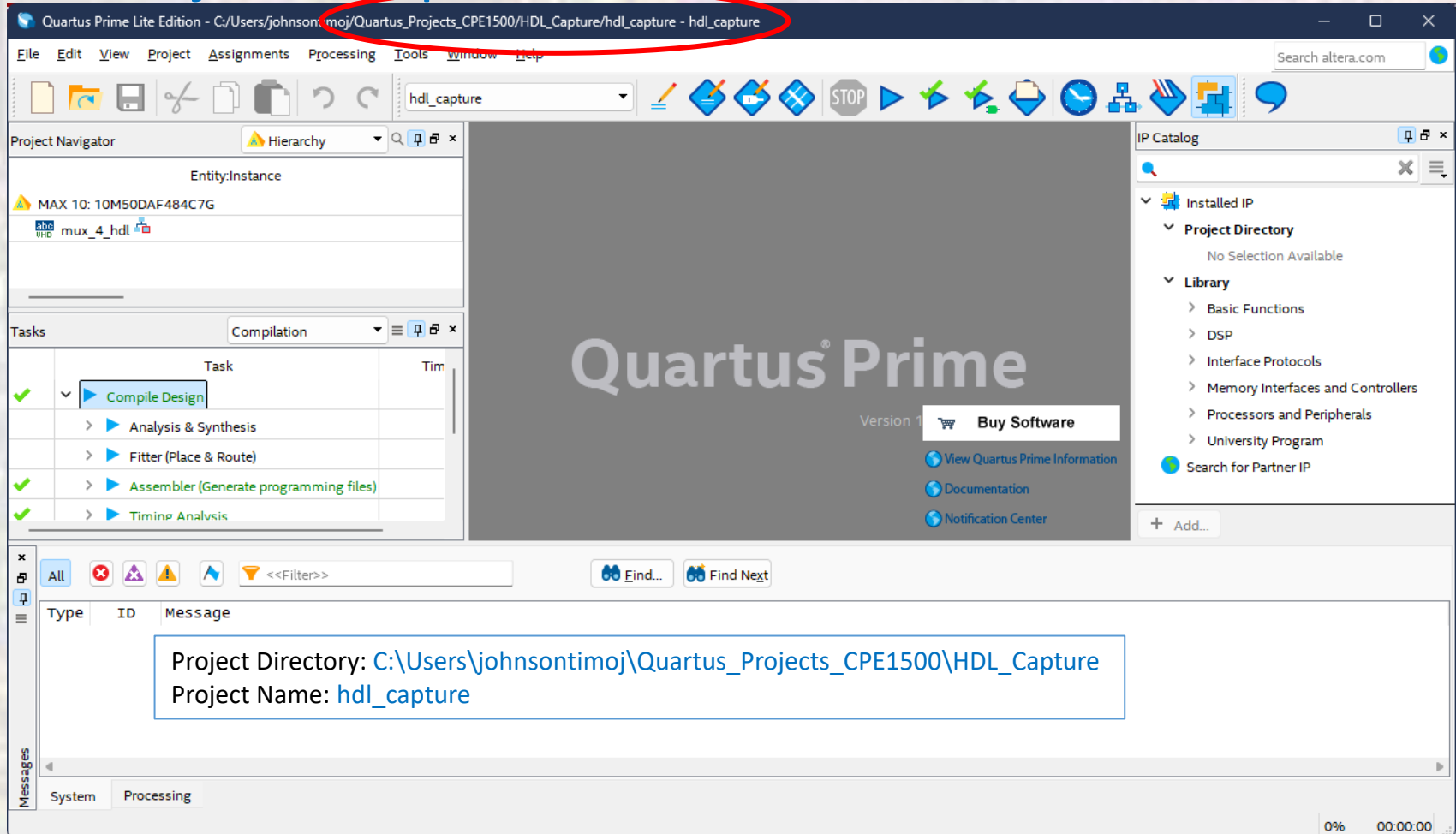
Last updated 1/13/25

VHDL Generation

- VHDL Design Capture
 - Process
 1. Create a new Quartus Project – see the [Quartus Project Setup](#) slides
 2. Open a new [VHDL](#) file(vhdl)
 3. Enter the VHDL code
 4. Set [Top Level Entity](#)
 5. Run [Analysis](#) to verify connectivity

Schematic Generation

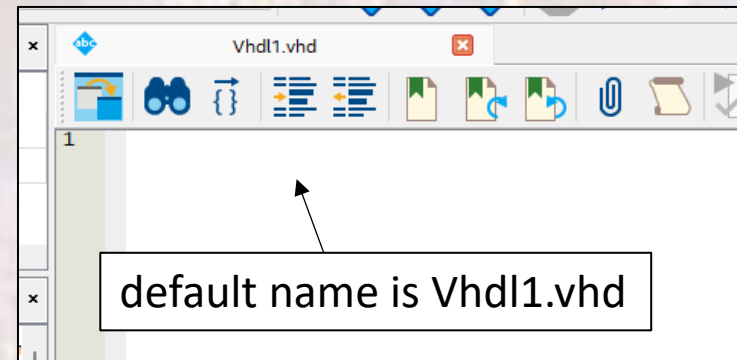
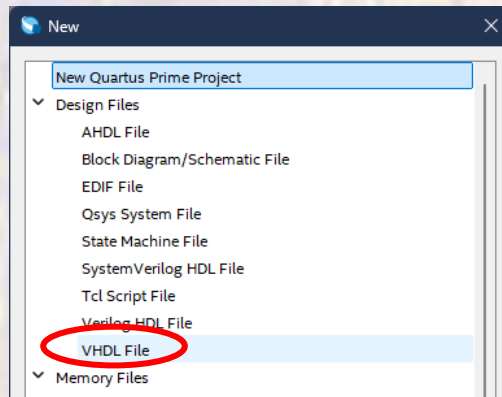
1. Create a new Quartus Project – see the [Quartus Project Setup](#) slides



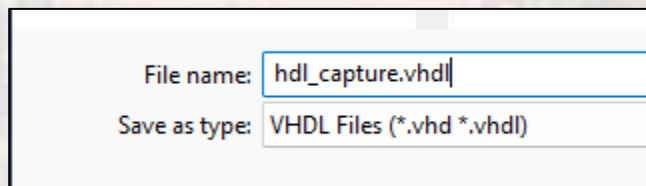
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2. Open a new VHDL file (BDF)

- File → New → VHDL File
- OK



- File → Save As
 - Change the name to a descriptive name
- Save



Be sure to use the
.vhdl file extension
.vhd means virtual
hard drive to Windows

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3. Enter Code

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows the VHDL code for a 4-to-1 multiplexer. The code is as follows:

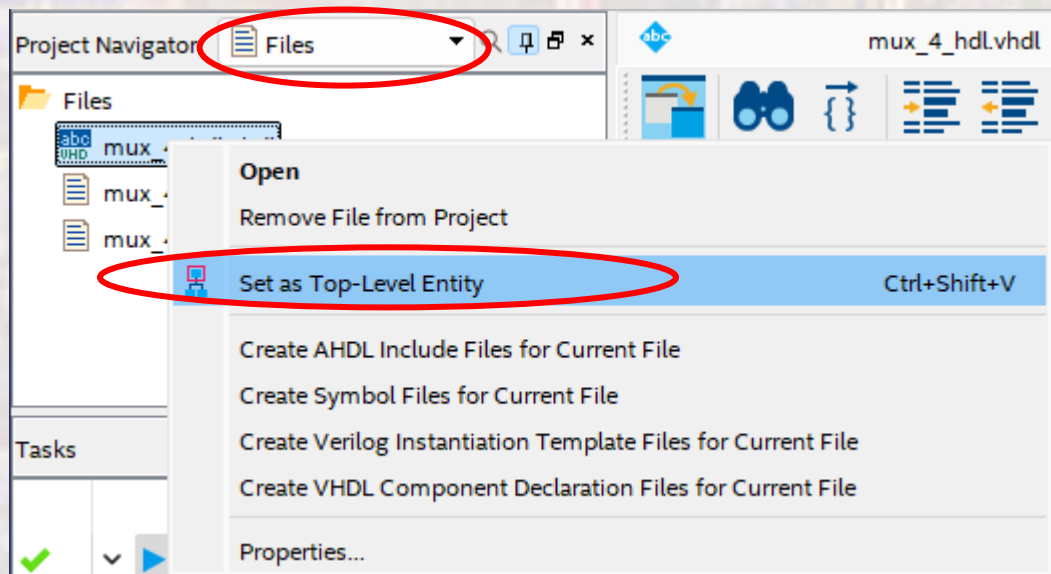
```
1  --  
2  -- mux_4_hdl.vhdl  
3  --  
4  -- created 12/18/24  
5  -- tj  
6  --  
7  -----  
8  --  
9  -- HDL version of a 4 to 1 mux  
10 --  
11 -----  
12 --  
13 -- inputs: a, b, c, d, sel0, sel1  
14 -- outputs: mux_out  
15 --  
16 -----  
17 library ieee;  
18 use ieee.std_logic_1164.all;  
19  
20 entity mux_4_hdl is  
21 port (  
22     i_a : in std_logic;  
23     i_b : in std_logic;  
24     i_c : in std_logic;  
25     i_d : in std_logic;  
26     i_sel : in std_logic_vector(1 downto 0);  
27  
28     o_mux_out : out std_logic
```

The interface includes a Project Navigator on the left showing the file structure, a Tasks pane with a compilation checklist, and an IP Catalog on the right. The status bar at the bottom indicates the current file is a VHDL File at line 1, column 1.

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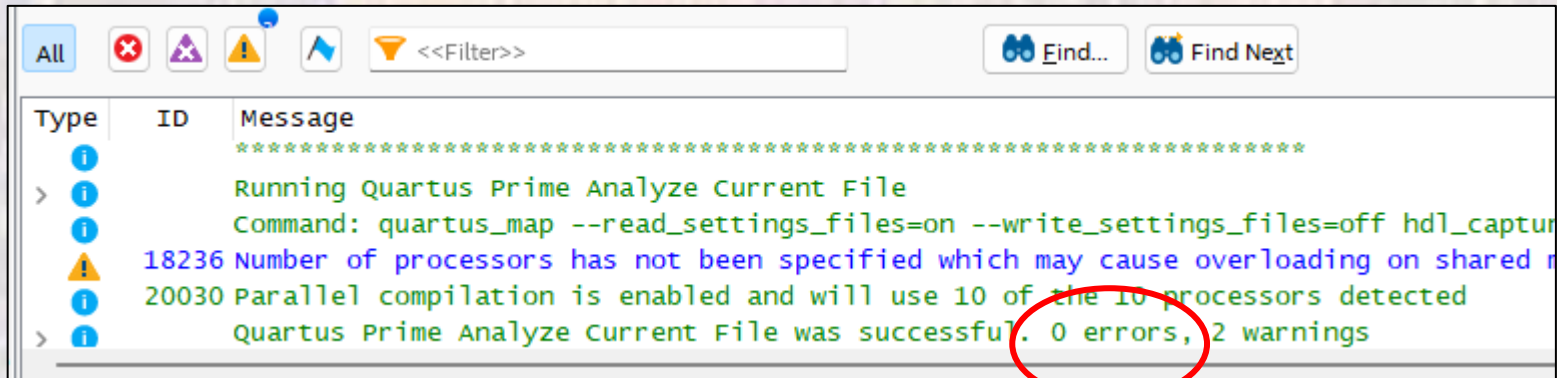
4. Set the Top Level Entity

- Select **Files**
- Rt-click on the design → **Set as Top Level Entity**



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5. Run Analysis to verify the connections
 - Processing → Analyze Current File



The screenshot shows the Messages window in Quartus Prime. The window has a toolbar with icons for All, Error, Warning, Info, and a Filter dropdown. The message list contains the following entries:

Type	ID	Message

>		Running Quartus Prime Analyze Current File
		Command: quartus_map --read_settings_files=on --write_settings_files=off hd1_captur
	18236	Number of processors has not been specified which may cause overloading on shared r
	20030	Parallel compilation is enabled and will use 10 of the 10 processors detected
>		Quartus Prime Analyze Current File was successful. 0 errors, 2 warnings

A red circle highlights the text "0 errors, 2 warnings" in the final message.