VHDL Generation

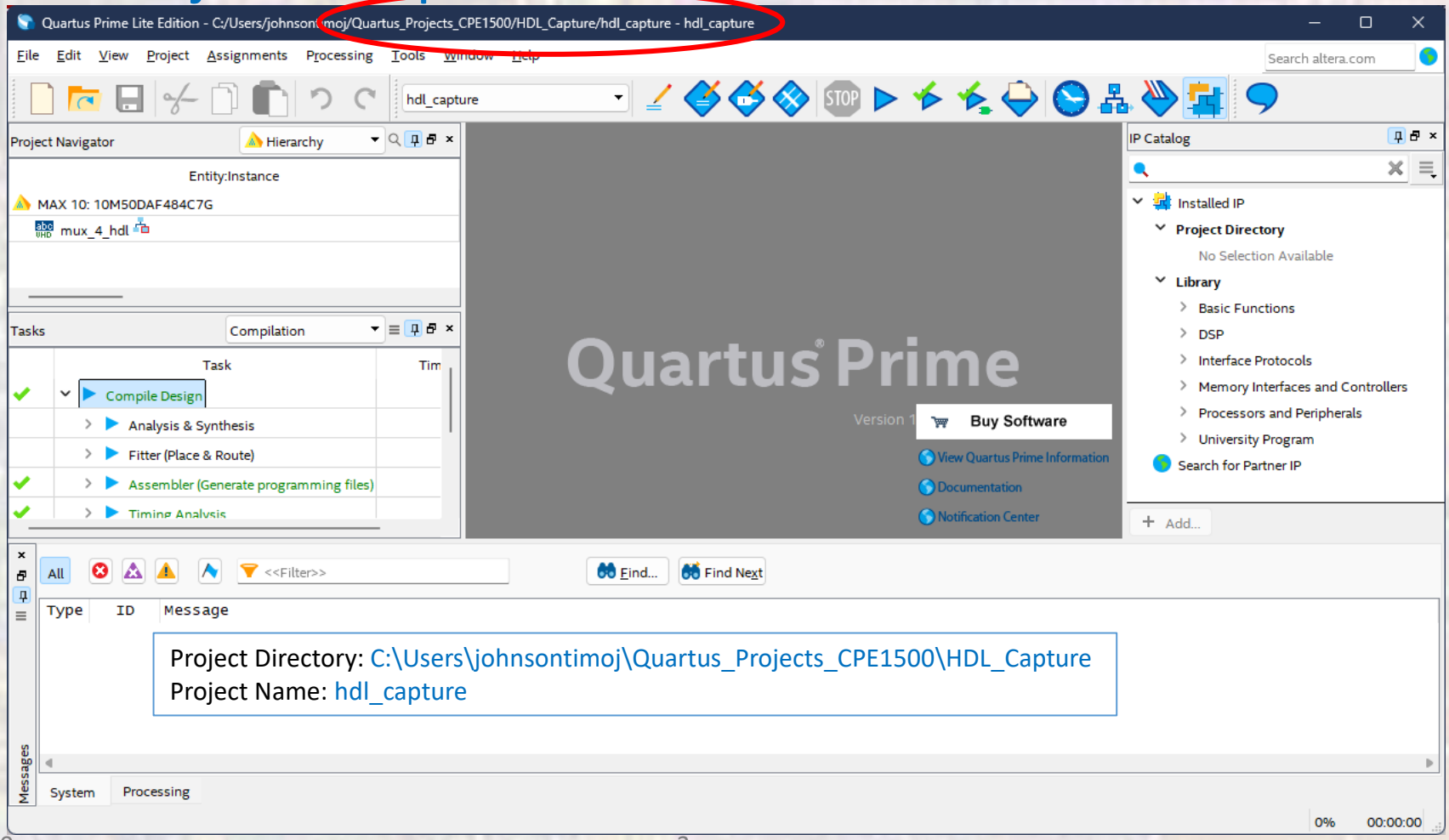
Last updated 1/13/25

VHDL Generation

- VHDL Design Capture
  - Process
    1. Create a new Quartus Project – see the Quartus Project Setup slides
    2. Open a new VHDL file(vhdl)
    3. Enter the VHDL code
    4. Set Top Level Entity
    5. Run Analysis to verify connectivity

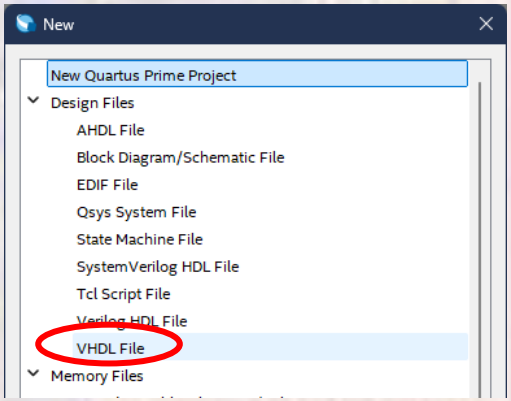
Schematic Generation

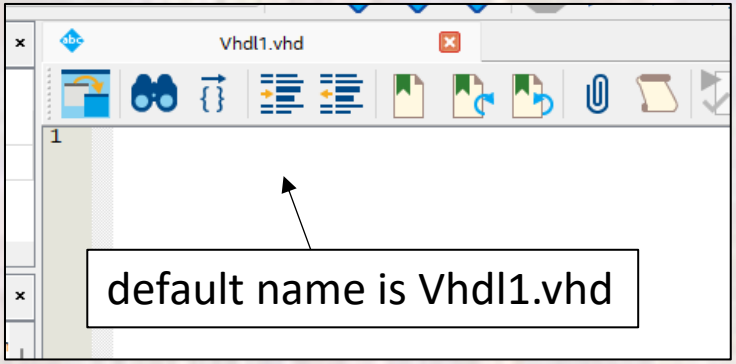
1. Create a new Quartus Project – see the Quartus Project Setup slides



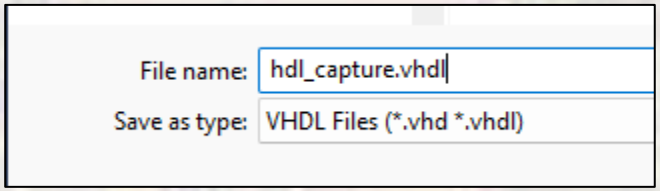
VHDL Generation

2. Open a new VHDL file (BDF)
   - File → New → VHDL File
   - OK





   - File → Save As
     - Change the name to a descriptive name
   - Save



Be sure to use the .vhdl file extension .vhd means virtual hard drive to Windows

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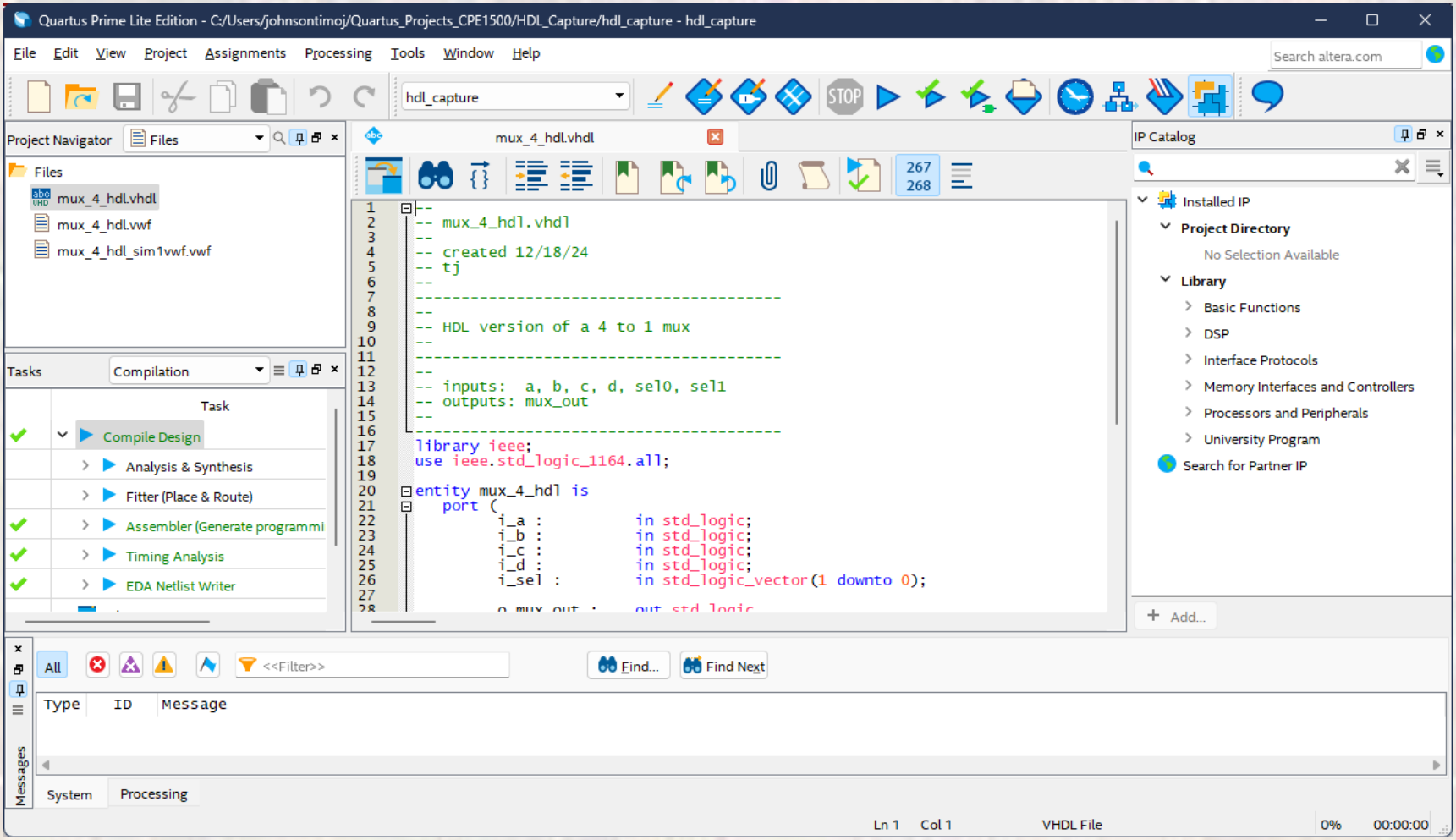
3. Enter Code



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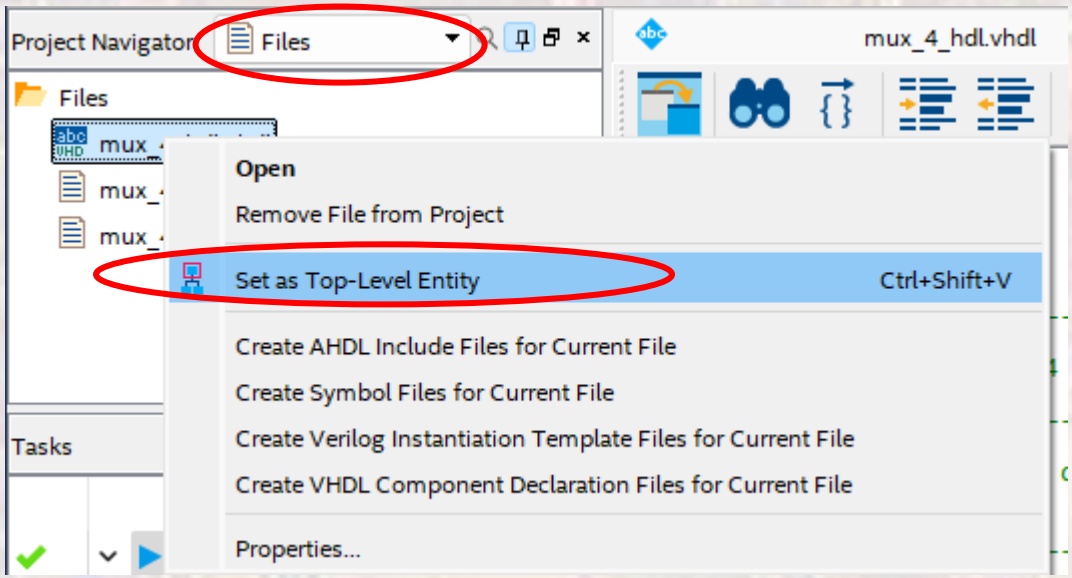
4. Set the Top Level Entity
   - Select Files
   - Rt-click on the design→ Set as Top Level Entity



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5. Run Analysis to verify the connections
   - Processing → Analyze Current File