Last updated 12/18/24

- Simulation using the University Waveform tool
 - 1. Create the HDL file(s)
 - 2. Run Analysis and Elaboration in Quartus
 - 3. Verify the RTL is what is expected
 - 4. Open a new University Program VWF file
 - 5. Select the desired signals to drive / analyze
 - 6. Setup the input signal waveforms
 - 7. Setup simulator options
 - 8. Run the simulation
 - 9. Evaluate the results

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1) Create the HDL file

mux_4_hdl.vhdl -- created 12/18/24 -- tj -- HDL version of a 4 to 1 mux -- inputs: a, b, c, d, sel0, sel1 -- outputs: mux_out library ieee; use ieee.std_logic_1164.all; entity mux_4_hdl is port (i_a : in std_logic; i_b : in std_logic; i_c : in std_logic; in std_logic; i_d : in std_logic_vector(1 downto 0); i_sel : out std_logic o_mux_out :); end entity; architecture behavioral of mux_4_hdl is internal signals - just for clarity signal a_int: std_logic; signal b_int: std_logic; signal c_int: std_logic; signal d_int: std_logic; begin o_mux_out <= a_int or b_int or c_int or d_int;</pre> end architecture;

- 2) Run Analysis and Synthesis in Quartus Creates a gate level implementation of the HDL
 - Set the top-level block
 - Rt-click on your top level block
 - Select Set as Top-level Entity

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2) Run Analysis and Synthesis in Quartus

- Processing → Start → Start Analysis and Synthesis
 - Check the Device
 - Check the Top-level Entity Name

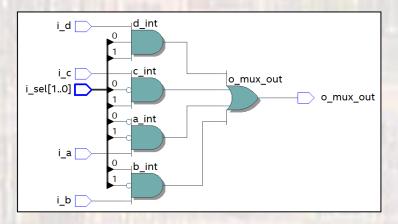
21057 Implemented 9 device resources after synthesis - the final resource count might be different Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings

Flow Summary	
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Flow Status	Successful - Wed Dec 18 14:15:35 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	hat_capture
Top-level Entity Name	mux_4_hdl
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Finat
Total logic elements	2
Total registers	0
Total pins	7
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

3) Verify the RTL (schematic of the implementation)

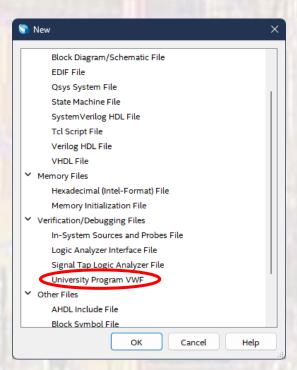
- Tools → Netlist Viewers → RTL Viewer
 - Evaluate the schematic does it make sense?

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4) Open a new University Program VWF file

File → New → University Program VWF



4) Open a new University Program VWF file

- File → New → University Program VWF
- Save the file: File \rightarrow Save As
 - Give is a useful file name (mux_4_hdl_sim1.vwf)

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5) Select the desired signals to drive / analyze

- Edit \rightarrow Insert Node or Bus
- Node Finder...
- List

At this point we will only see the pins

Inper Input adue type: 9-Level Binary Node Finder Index Finder Input Input
width: 1 1 0

5) Select the desired signals to drive / analyze

- Use the arrows to move nodes form the Found list to the Selected list
- OK, OK

🕤 Node Finder		×	🕥 Node Finder	Х
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6) Setup the input signal waveforms

- You must have a plan
 - What signals to switch at what time
 - How long does the total test take
- Edit \rightarrow Set Grid Size (10 ns)
- Edit → Set End Time (640 ns)

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6) Setup the input signal waveforms

- See the University Waveform Viewer Input Setup Slides (lab 2)
- File \rightarrow Save

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7) Setup the simulator options

- Simulation → Simulation Settings
- Select VHDL
- Verify the vwf file name
 - If incorrect Restore Defaults
- Save

Caution: Improv	edy modifying these settings can cause the simulation to fail
. Language: 🔿 Veril 😦 🗿 VH	DL The language used for the testbench and netlist)
unctional Simulation Settings	Timing Simulation Settings
estbench Generation Command	(Functional Simulation):
juartus_edagen_testbencht	tool=modelsim_oemformat=vhdlwrite_settings_files=off hdl_capture -c h
etlist Generation Command (Fu	nctional Simulation):
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onerror {exit -code 1}	
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vcd file -direction hdl_capture.m	/sim.vcd
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8) Run Simulation

• Simulation → Run Functional Simulation

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9) Evaluate results

Compare simulation results with expected results

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in —	i_sel	во					
in —	i_sel	во					
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