

HDL Simulations University Waveforms

Last updated 12/18/24

HDL Simulation – University Waveforms

- Simulation using the University Waveform tool
 1. Create the HDL file(s)
 2. Run **Analysis and Elaboration** in Quartus
 3. Verify the RTL is what is expected
 4. Open a new **University Program VWF** file
 5. Select the desired signals to drive / analyze
 6. Setup the input signal waveforms
 7. Setup simulator options
 8. Run the simulation
 9. Evaluate the results

HDL Simulation – University Waveforms

1) Create the HDL file

```
--
-- mux_4_hdl.vhd1
-- created 12/18/24
-- tj
--
-----
-- HDL version of a 4 to 1 mux
--
-----
-- inputs: a, b, c, d, sel0, sel1
-- outputs: mux_out
--
-----
library ieee;
use ieee.std_logic_1164.all;

entity mux_4_hdl is
  port (
    i_a :      in std_logic;
    i_b :      in std_logic;
    i_c :      in std_logic;
    i_d :      in std_logic;
    i_sel :    in std_logic_vector(1 downto 0);
    o_mux_out : out std_logic
  );
end entity;

architecture behavioral of mux_4_hdl is
  -- internal signals - just for clarity
  signal a_int: std_logic;
  signal b_int: std_logic;
  signal c_int: std_logic;
  signal d_int: std_logic;

begin
  a_int <= i_a and not i_sel(1) and not i_sel(0);
  b_int <= i_b and not i_sel(1) and i_sel(0);
  c_int <= i_c and i_sel(1) and not i_sel(0);
  d_int <= i_d and i_sel(1) and i_sel(0);

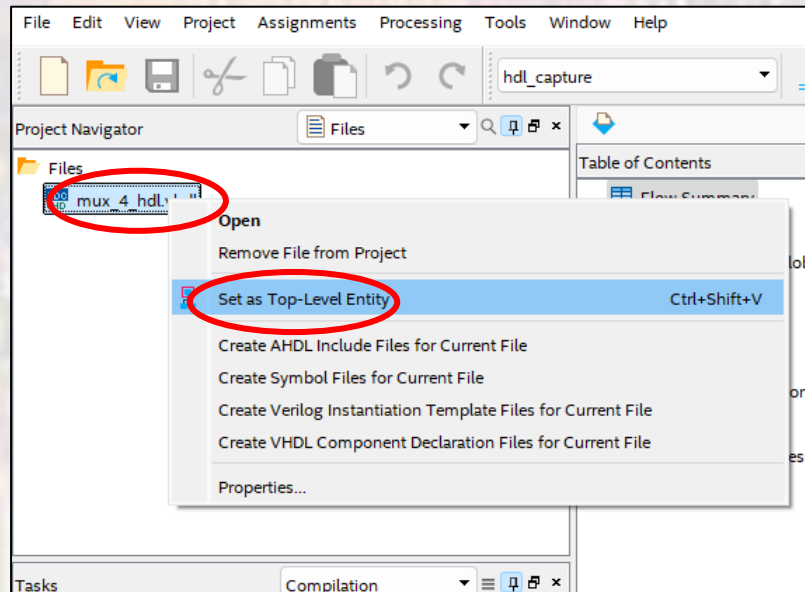
  o_mux_out <= a_int or b_int or c_int or d_int;
end architecture;
```

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2) Run Analysis and Synthesis in Quartus

Creates a gate level implementation of the HDL

- Set the top-level block
 - Rt-click on your top level block
 - Select **Set as Top-level Entity**

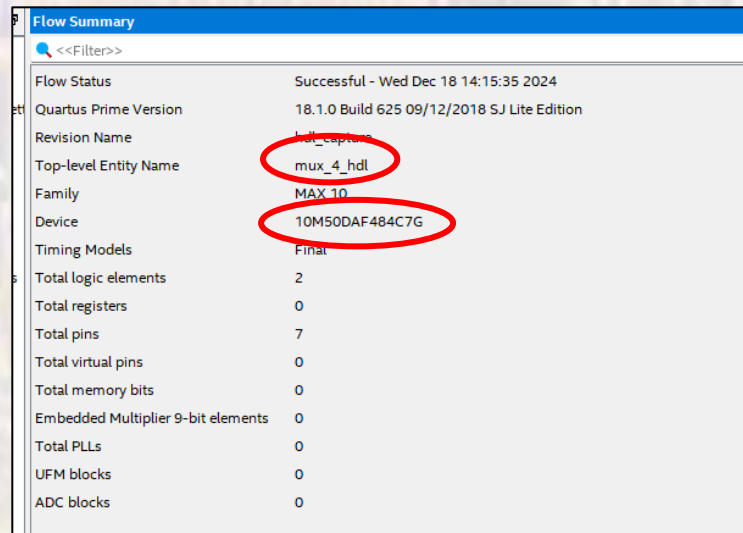


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2) Run Analysis and Synthesis in Quartus

- Processing → Start → Start Analysis and Synthesis
 - Check the Device
 - Check the Top-level Entity Name

21057 Implemented 9 device resources after synthesis - the final resource count might be different
quartus prime analysis & synthesis was successful. 0 errors, 2 warnings



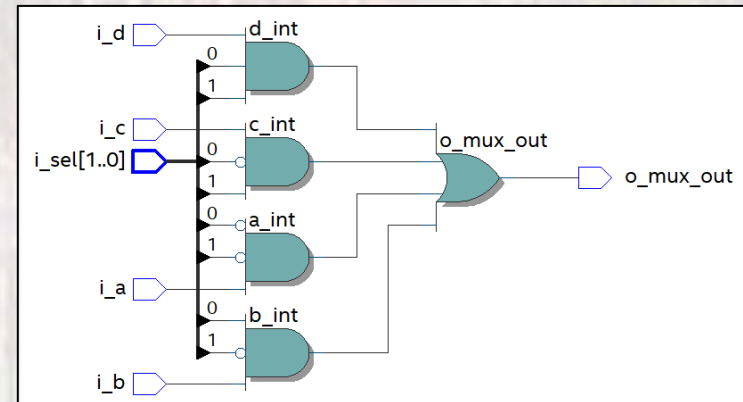
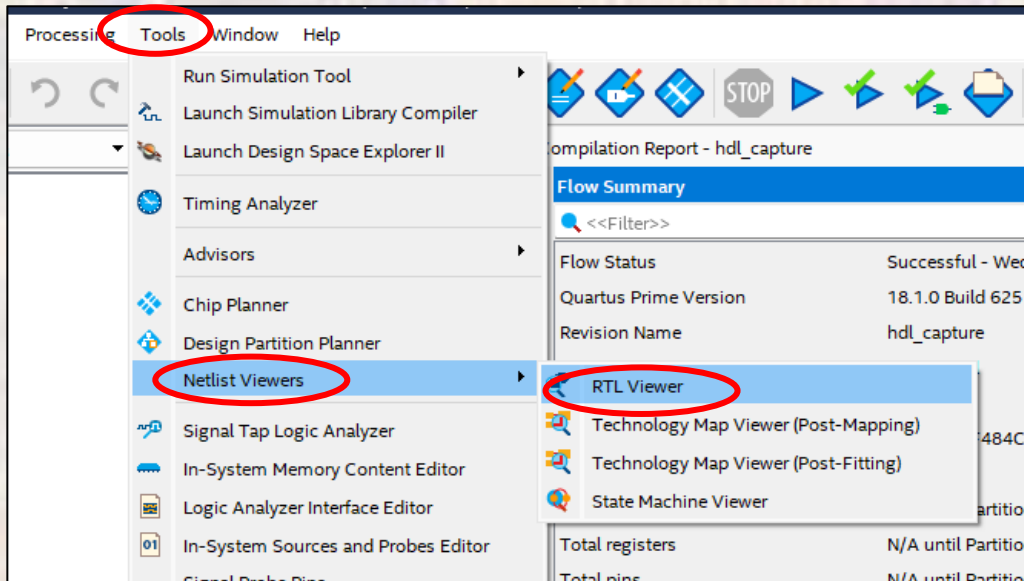
The screenshot shows the 'Flow Summary' window in Quartus. The 'Flow Status' is 'Successful - Wed Dec 18 14:15:35 2024'. The 'Top-level Entity Name' is 'mux_4_hdl' and the 'Device' is '10M50DAF484C7G', both of which are circled in red. The 'Device' field also includes 'MAX 10' in parentheses. Other fields include 'Revision Name' (hdl_capture), 'Timing Models' (Final), and various resource counts (Total logic elements: 2, Total registers: 0, Total pins: 7, Total virtual pins: 0, Total memory bits: 0, Embedded Multiplier 9-bit elements: 0, Total PLLs: 0, UFM blocks: 0, ADC blocks: 0).

Property	Value
Flow Status	Successful - Wed Dec 18 14:15:35 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	hdl_capture
Top-level Entity Name	mux_4_hdl
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2
Total registers	0
Total pins	7
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

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3) Verify the RTL (schematic of the implementation)

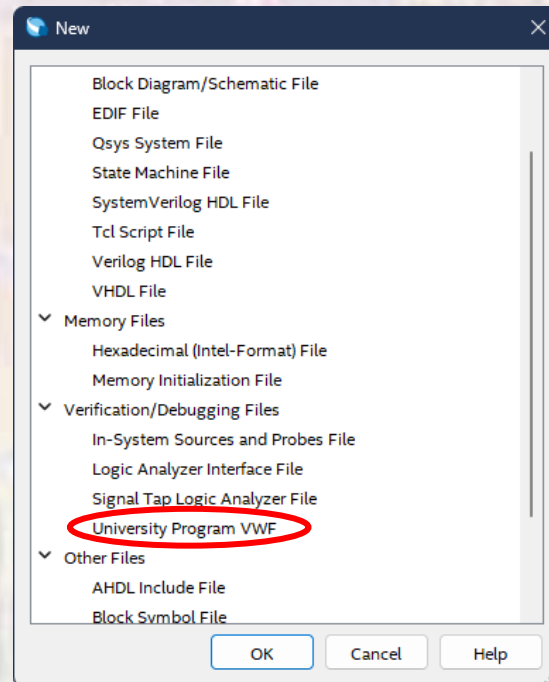
- Tools → Netlist Viewers → RTL Viewer
- Evaluate the schematic – does it make sense?



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4) Open a new University Program VWF file

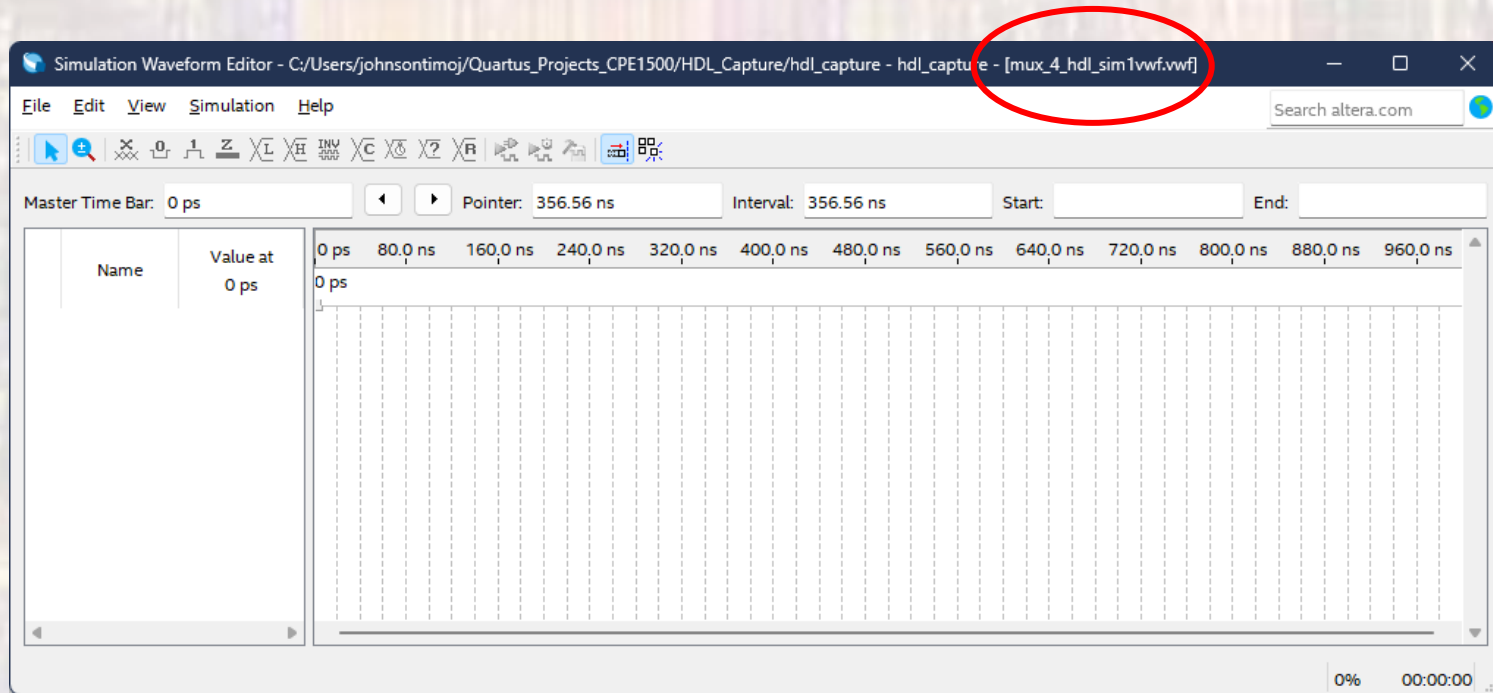
- File → New → University Program VWF



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4) Open a new University Program VWF file

- File → New → University Program VWF
- Save the file: File → Save As
 - Give is a useful file name (mux_4_hdl_sim1.vwf)

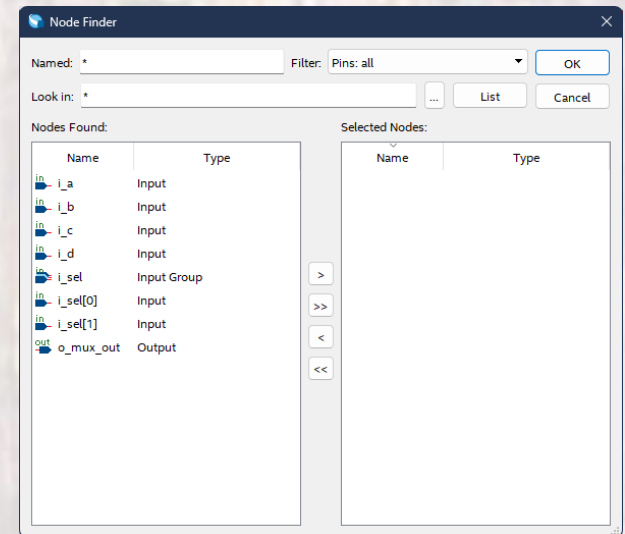
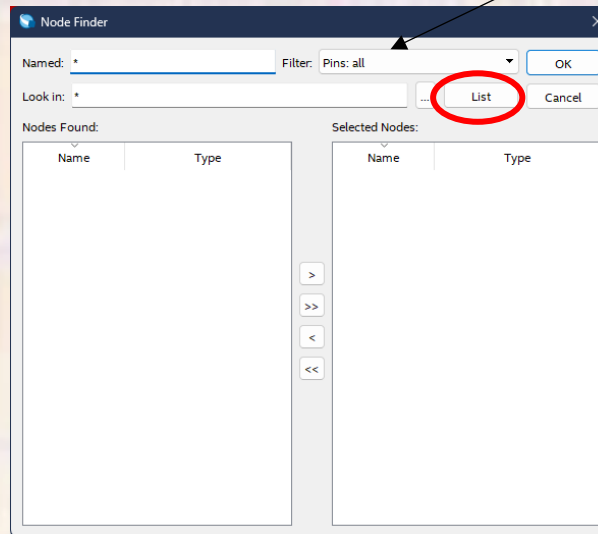
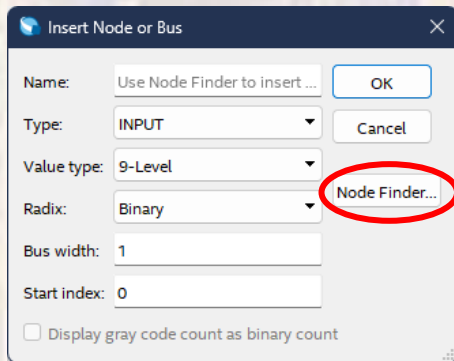


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5) Select the desired signals to drive / analyze

- Edit → Insert Node or Bus
- Node Finder...
- List

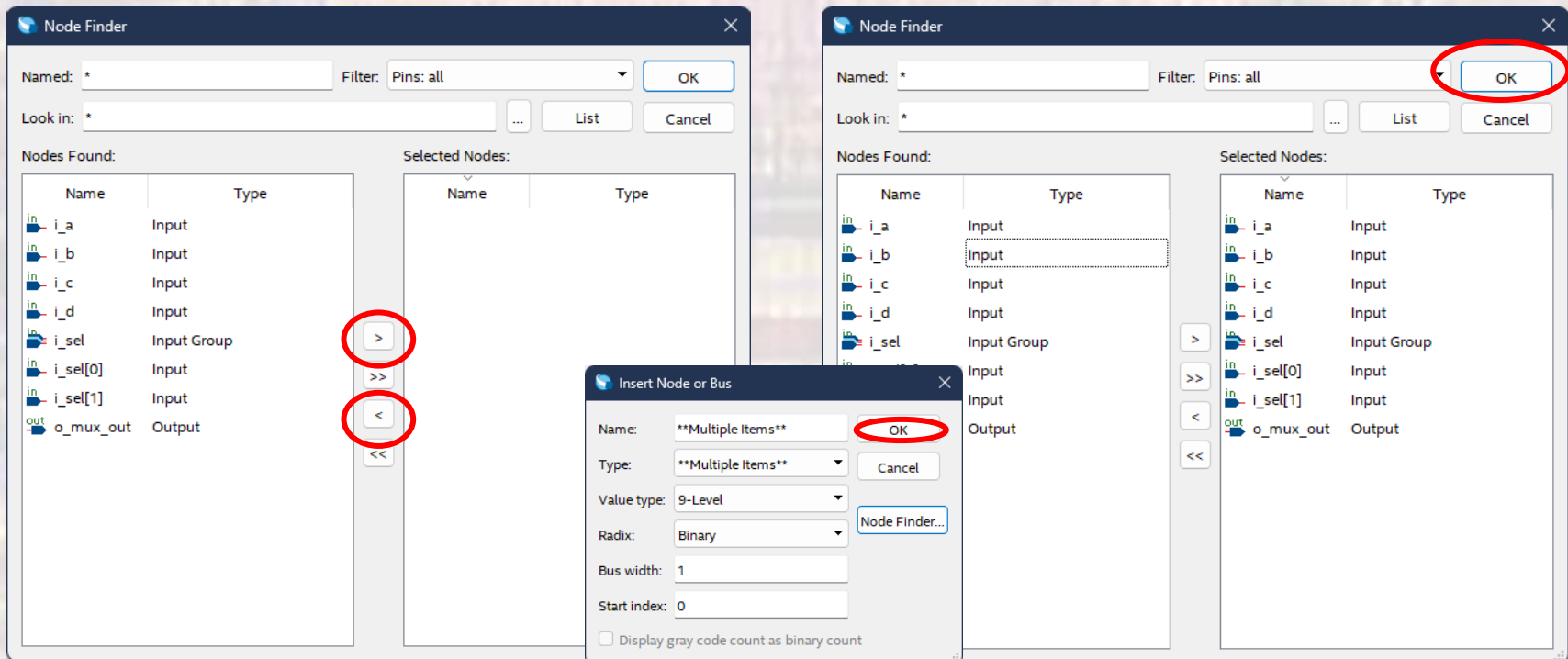
At this point we will only see the pins



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5) Select the desired signals to drive / analyze

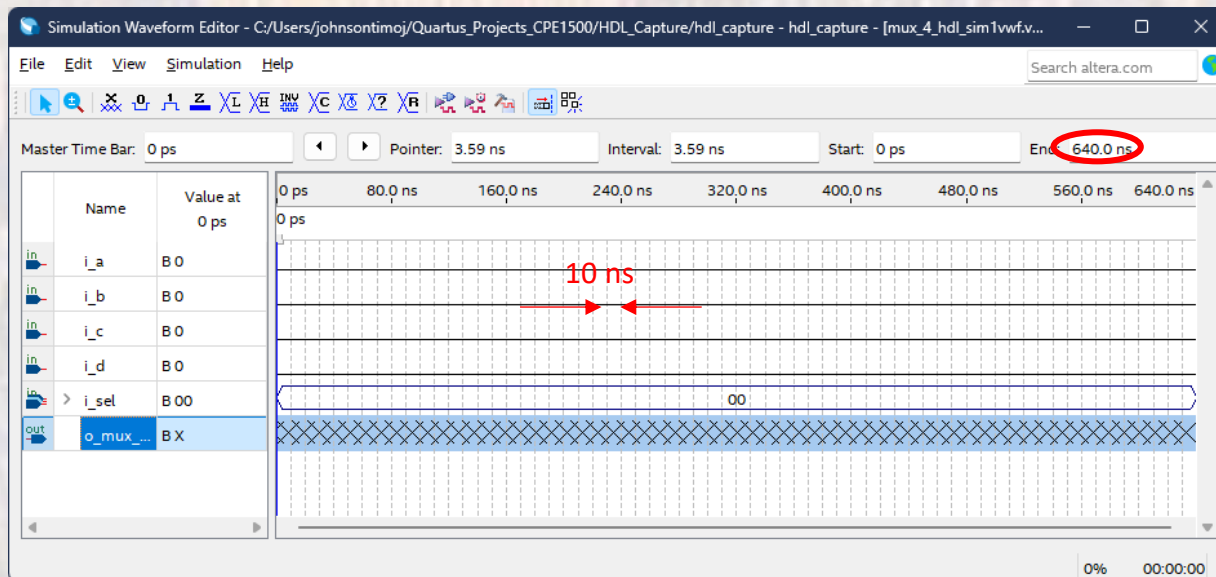
- Use the arrows to move nodes from the Found list to the Selected list
- OK, OK



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6) Setup the input signal waveforms

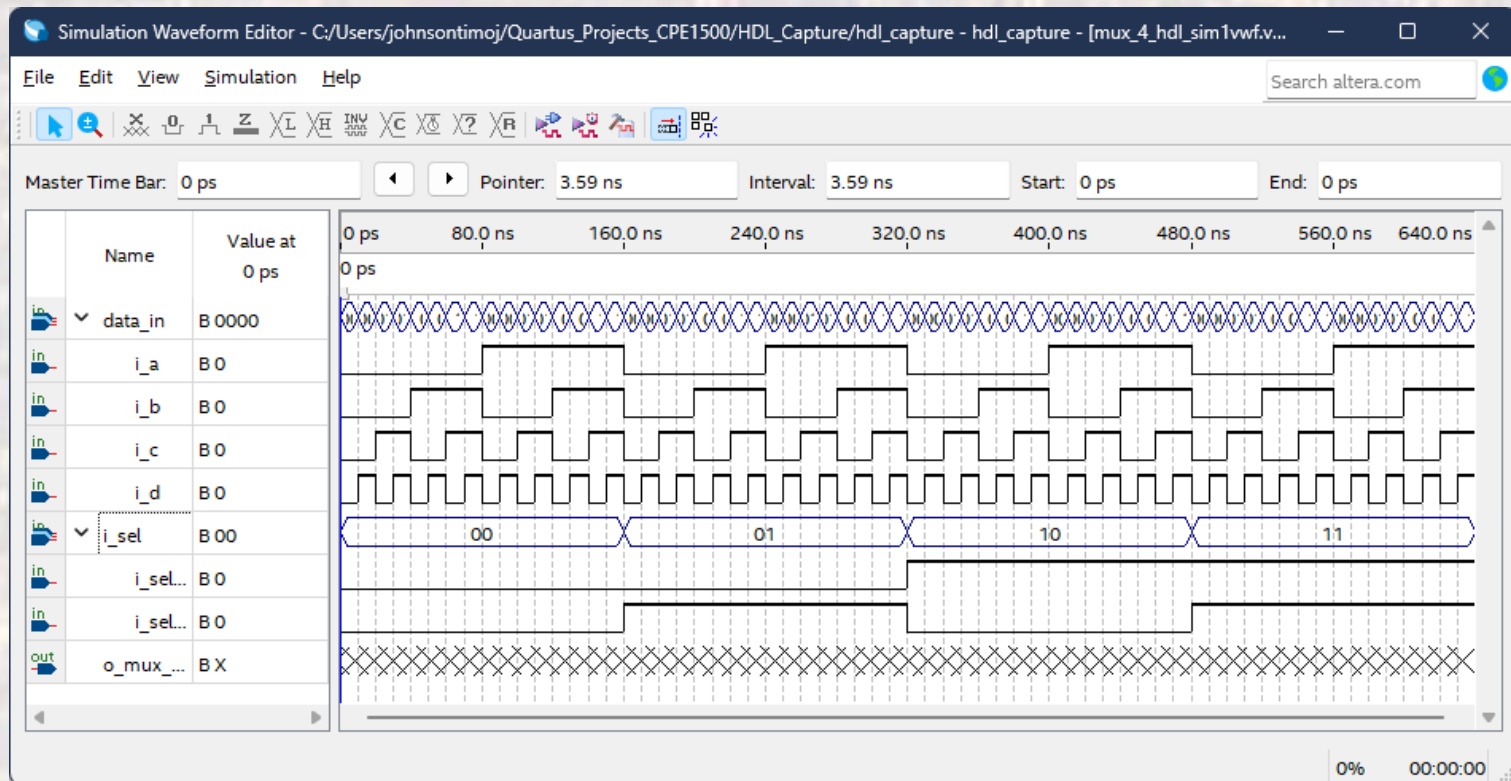
- You must have a plan
 - What signals to switch at what time
 - How long does the total test take
- **Edit** → **Set Grid Size** (10 ns)
- **Edit** → **Set End Time** (640 ns)



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6) Setup the input signal waveforms

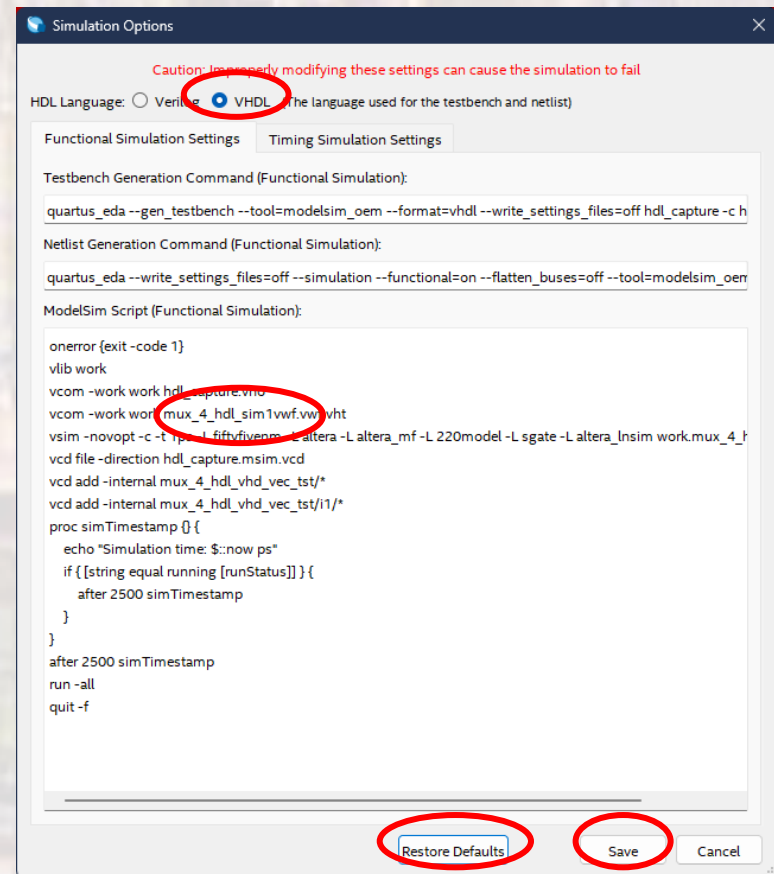
- See the [University Waveform Viewer – Input Setup Slides](#) (lab 2)
- **File** → **Save**



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7) Setup the simulator options

- Simulation → Simulation Settings
- Select VHDL
- Verify the vwf file name
 - If incorrect Restore Defaults
- Save



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8) Run Simulation

- Simulation → Run Functional Simulation

The image shows two overlapping windows from the Quartus software. The left window, titled 'Simulation Flow Progress', displays the status of the simulation process. A green progress bar at the top indicates that the simulation is complete. Below the progress bar, a text box contains the text 'Run Log (Will show any errors) (Disappears if all ok)'. The main text area shows the command 'write_settings_files=off lab1 -c lab1 --' and the status 'Completed successfully.' followed by a green checkmark. Below this, there is a section titled '**** Generating the functional simulation netlist ****' and a list of command-line options for the simulation tool.

The right window, titled 'Simulation Waveform Editor', shows a timing diagram. The top menu bar includes 'File', 'Edit', 'View', 'Simulation', and 'Help'. The toolbar contains various icons for navigation and analysis. The 'Master Time Bar' is set to '0 ps' and the 'Pointer' is at '105.83 ns'. The 'Interval' is set to '160,0 ns'. The waveform plot shows several signals: 'data_in' (a constant high signal), 'i_a', 'i_b', 'i_c', and 'i_d' (square waves), 'i_sel' (a signal with values 00, 01, 10, and 11), and 'o_mux_...' (a square wave). A text box on the right side of the waveform plot contains the text 'Simulation Plot (not the VWF window)'. The bottom status bar shows '0%' and '00:00:00'.

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9) Evaluate results

- Compare simulation results with expected results

