

# VHDL to DE10

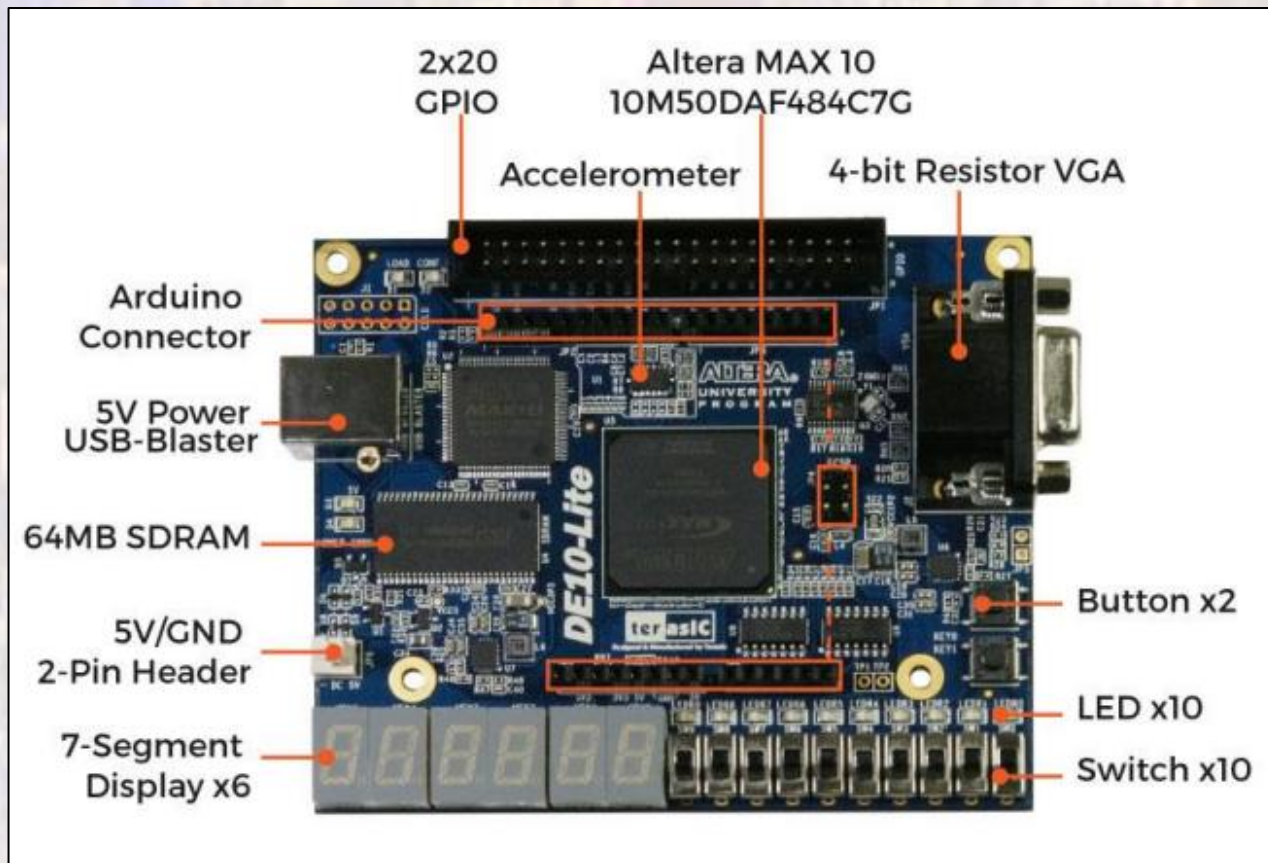
Last updated 1/14/25

# VHDL to DE10

- Verification via Hardware (DE10)
  1. Create the VHDL
  2. Verify the design via simulation
    - see the [VHDL Simulation University Waveforms](#) slides
  3. Plan the DE10 locations for each pin on the schematic
  4. Map the VHDL pins to DE10 inputs and outputs
  5. Compile the design
  6. Download the design to the DE10
  7. Verify the design

# VHDL to DE10

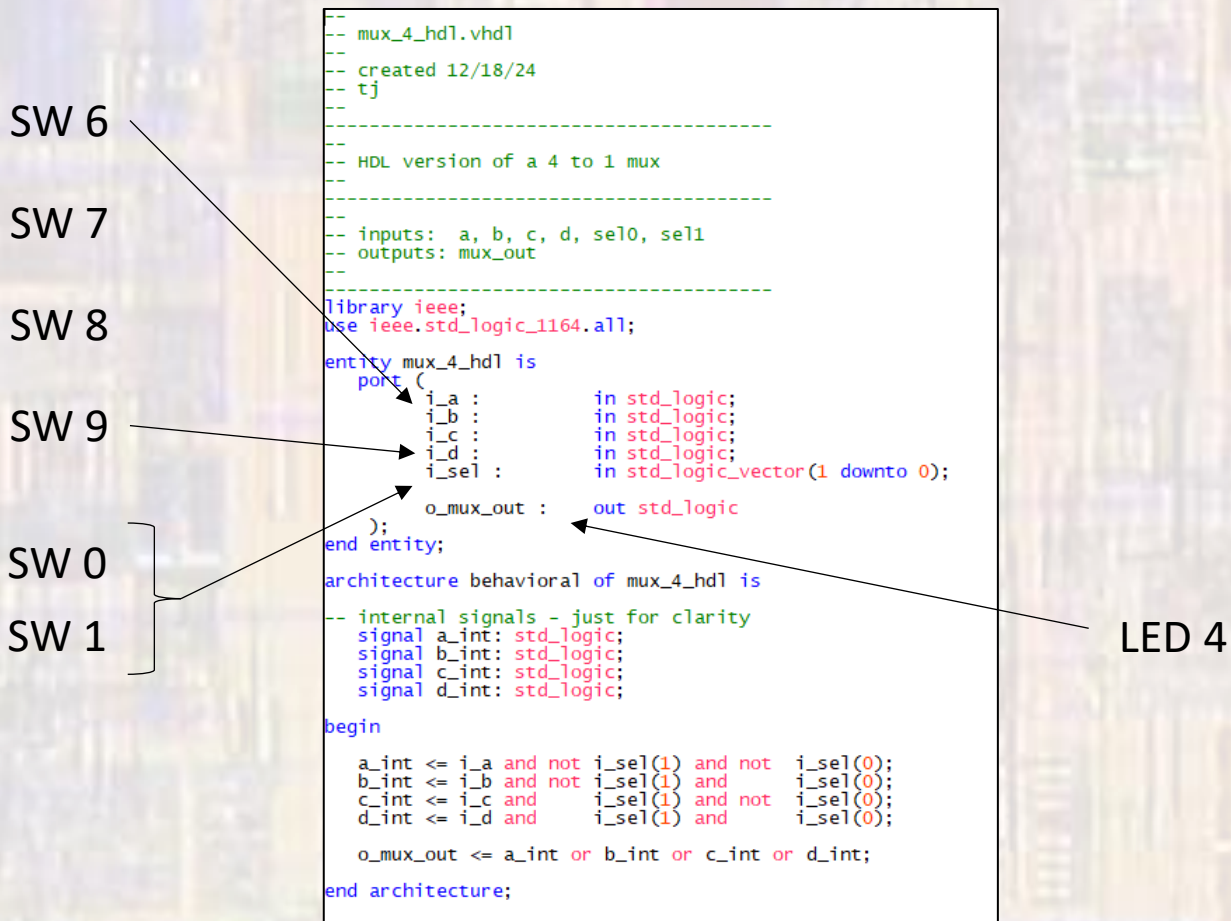
3) Plan the DE10 locations for each pin on the schematic



9 SW and LED 0

# VHDL to DE10

## 3) Plan the DE10 locations for each pin on the schematic



# VHDL to DE10

## 4) Map the schematic pins to DE10 inputs and outputs

sel0  
sel1

a  
b  
c  
d

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTTL

mux\_out

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTTL

# VHDL to DE10

## 4) Map the schematic pins to DE10 inputs and outputs

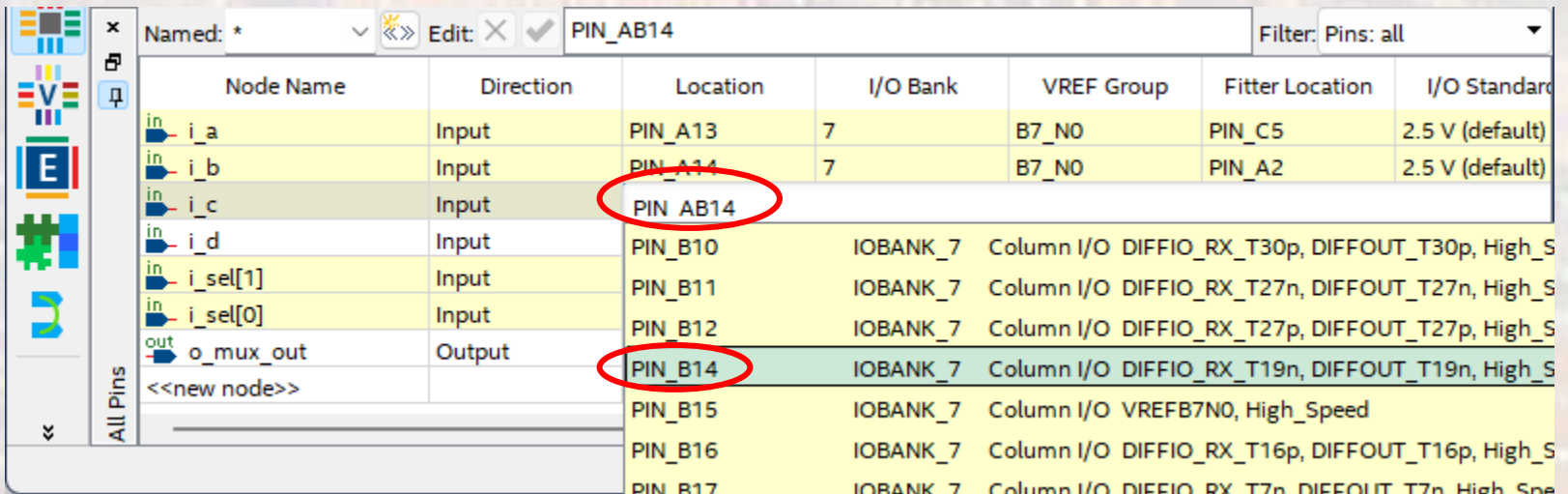
- Assignments → Pin Planner

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
i_a	Input				PIN_C5	2.5 V (default)
i_b	Input				PIN_A2	2.5 V (default)
i_c	Input				PIN_B3	2.5 V (default)
i_d	Input				PIN_B5	2.5 V (default)
i_sel[1]	Input				PIN_B4	2.5 V (default)
i_sel[0]	Input				PIN_A3	2.5 V (default)
o_mux_out	Output				PIN_F7	2.5 V (default)
<<new node>>						

# VHDL to DE10

## 4) Map the schematic pins to DE10 inputs and outputs

- Double click on the location column for a pin
- Select the expand arrow
- Scroll until the desired pin is found and select it
- Close the Pin Planner when finished



Named: \* Edit: PIN\_AB14 Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in i_a	Input	PIN_A13	7	B7_NO	PIN_C5	2.5 V (default)
in i_b	Input	PIN_A14	7	B7_NO	PIN_A2	2.5 V (default)
in i_c	Input	PIN_AB14				
in i_d	Input	PIN_B10	IOBANK_7	Column I/O	DIFFIO_RX_T30p, DIFFOUT_T30p, High_S	
in i_sel[1]	Input	PIN_B11	IOBANK_7	Column I/O	DIFFIO_RX_T27n, DIFFOUT_T27n, High_S	
in i_sel[0]	Input	PIN_B12	IOBANK_7	Column I/O	DIFFIO_RX_T27p, DIFFOUT_T27p, High_S	
out o_mux_out	Output	PIN_B14	IOBANK_7	Column I/O	DIFFIO_RX_T19n, DIFFOUT_T19n, High_S	
<<new node>>						
		PIN_B15	IOBANK_7	Column I/O	VREFB7N0, High_Speed	
		PIN_B16	IOBANK_7	Column I/O	DIFFIO_RX_T16p, DIFFOUT_T16p, High_S	
		PIN_B17	IOBANK_7	Column I/O	DIFFIO_RX_T7n, DIFFOUT_T7n, High_S	

# VHDL to DE10

## 5) Compile the design

- Save
- Right click on the design and select Set as Top-Level Entity
- Processing → Start Compilation
- Verify success

Flow Summary	
Search <<Filter>>	
Flow Status	Successful - Tue Jan 14 13:59:59 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	hdl_capture
Top-level Entity Name	mux_4_hdl
Family	10M50DAF484C7G
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	3 / 49,760 (< 1 %)
Total registers	0
Total pins	7 / 360 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

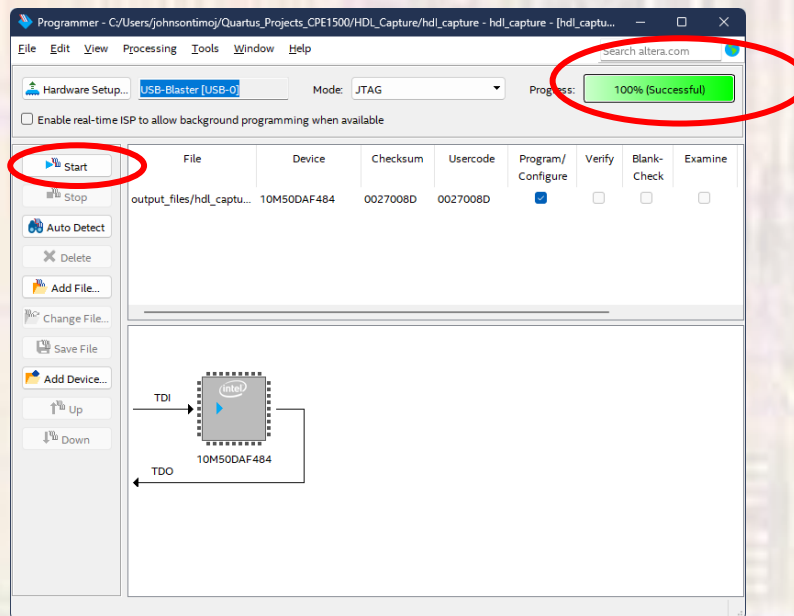
```
10905 Generated the EDA functional simulation netlist because it is the only supported netlist ty
204019 Generated file hdl_capture.vho in folder "C:/Users/johnsontimoj/Quartus_Projects_CPE1500/HDL
> 293000 Quartus Prime Full compilation was successful 0 errors, 19 warnings
```



# VHDL to DE10

## 6) Download the design to the DE10

- Plug the DE10 board into your laptop USB port
  - Should be lots of flashing lights
- **Tools** → **Programmer**
  - The USB Blaster interface should have been setup when you setup Quartus – see Quartus Setup Slides if it is not visible
- **Start**



# VHDL to DE10

## 7) Verify the design

- Choose a value for SW1 and SW0 (SEL(1) and SEL(0))
- Verify only the associated SW(9-6) toggle the LED on/off