VHDL to DE10

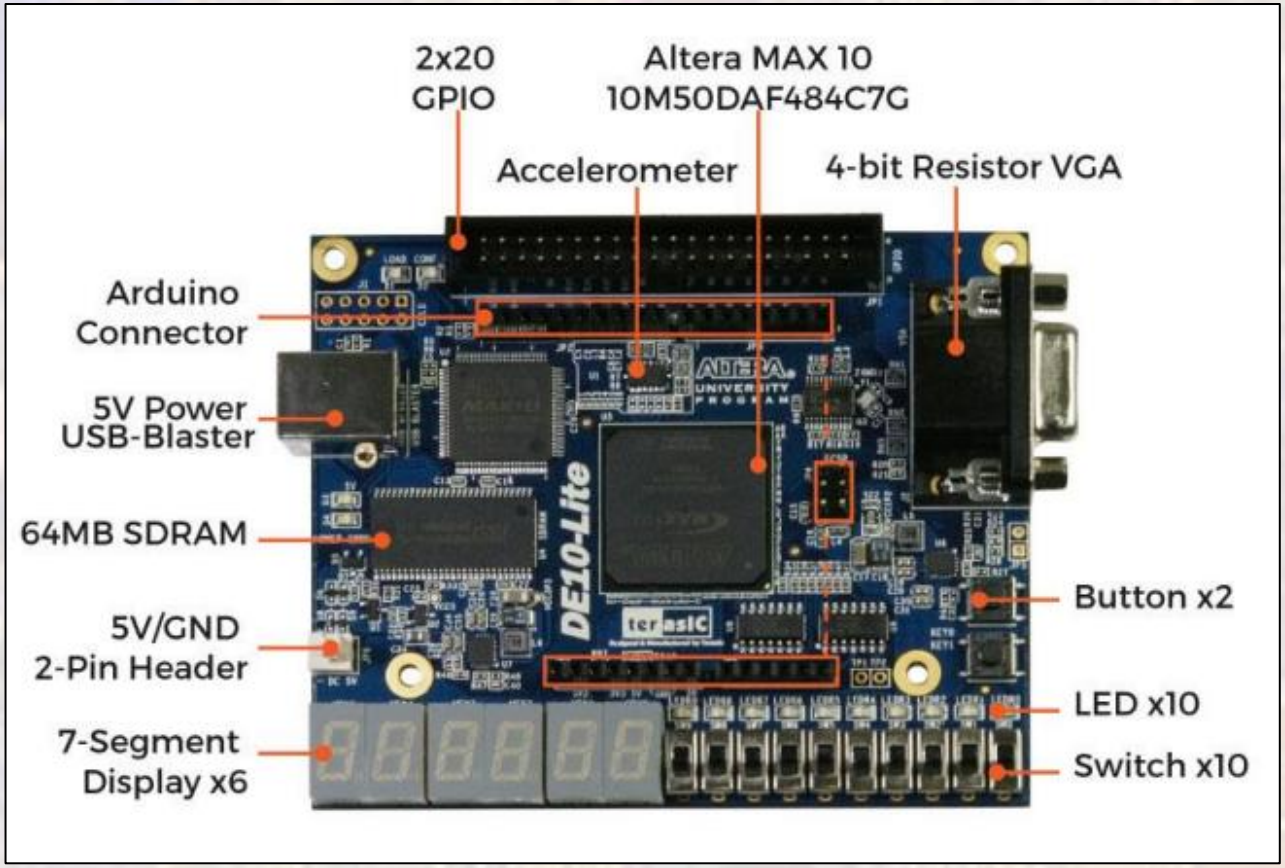
Last updated 1/14/25

VHDL to DE10

- Verification via Hardware (DE10)
  1. Create the VHDL
  2. Verify the design via simulation
     - see the VHDL Simulation University Waveforms slides
  3. Plan the DE10 locations for each pin on the schematic
  4. Map the VHDL pins to DE10 inputs and outputs
  5. Compile the design
  6. Download the design to the DE10
  7. Verify the design

VHDL to DE10

3) Plan the DE10 locations for each pin on the schematic



9 SW and LED 0

VHDL to DE10

3) Plan the DE10 locations for each pin on the schematic

SW 6

SW 7

SW 8

SW 9

SW 0

SW 1

```
--
-- mux_4_hdl.vhdl
--
-- created 12/18/24
-- tj
--
----------------------------------------
--
-- HDL version of a 4 to 1 mux
--
----------------------------------------
--
-- inputs:  a, b, c, d, sel0, sel1
-- outputs: mux_out
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity mux_4_hdl is
   port (
         i_a :          in std_logic;
         i_b :          in std_logic;
         i_c :          in std_logic;
         i_d :          in std_logic;
         i_sel :        in std_logic_vector(1 downto 0);

         o_mux_out :    out std_logic
   );
end entity;

architecture behavioral of mux_4_hdl is

-- internal signals - just for clarity
   signal a_int: std_logic;
   signal b_int: std_logic;
   signal c_int: std_logic;
   signal d_int: std_logic;

begin

   a_int <= i_a and not i_sel(1) and not  i_sel(0);
   b_int <= i_b and not i_sel(1) and      i_sel(0);
   c_int <= i_c and     i_sel(1) and not  i_sel(0);
   d_int <= i_d and     i_sel(1) and      i_sel(0);

   o_mux_out <= a_int or b_int or c_int or d_int;

end architecture;
```

LED 4

VHDL to DE10

4) Map the schematic pins to DE10 inputs and outputs

Table 3-4 Pin Assignment of Slide Switches

	Signal Name	FPGA Pin No.	Description	I/O Standard
sel0	SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTL
sel1	SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTL
	SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTL
	SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTL
	SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTL
	SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTL
a	SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTL
b	SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTL
c	SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTL
d	SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTL

Table 3-5 Pin Assignment of LEDs

	Signal Name	FPGA Pin No.	Description	I/O Standard
	LEDR0	PIN_A8	LED [0]	3.3-V LVTTL
	LEDR1	PIN_A9	LED [1]	3.3-V LVTTL
	LEDR2	PIN_A10	LED [2]	3.3-V LVTTL
	LEDR3	PIN_B10	LED [3]	3.3-V LVTTL
	LEDR4	PIN_D13	LED [4]	3.3-V LVTTL
mux_out	LEDR5	PIN_C13	LED [5]	3.3-V LVTTL
	LEDR6	PIN_E14	LED [6]	3.3-V LVTTL
	LEDR7	PIN_D14	LED [7]	3.3-V LVTTL
	LEDR8	PIN_A11	LED [8]	3.3-V LVTTL
	LEDR9	PIN_B11	LED [9]	3.3-V LVTTL

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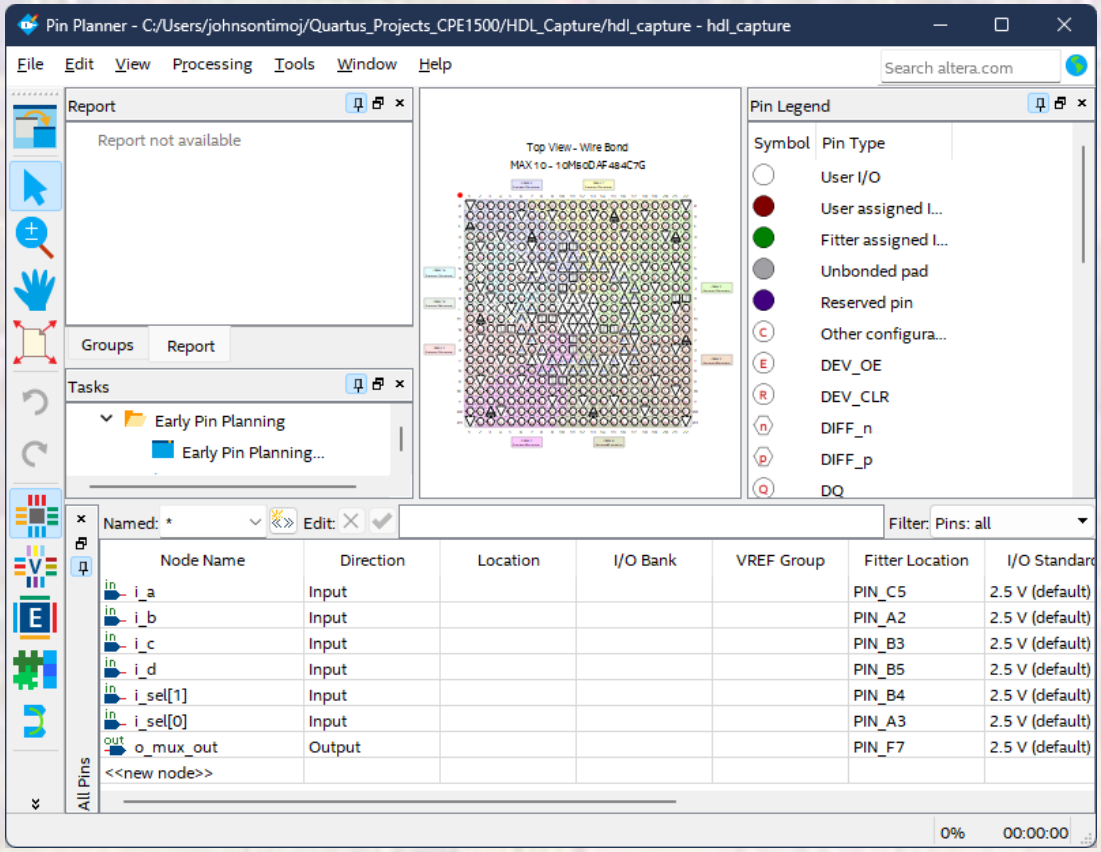
4) Map the schematic pins to DE10 inputs and outputs

- Assignments → Pin Planner



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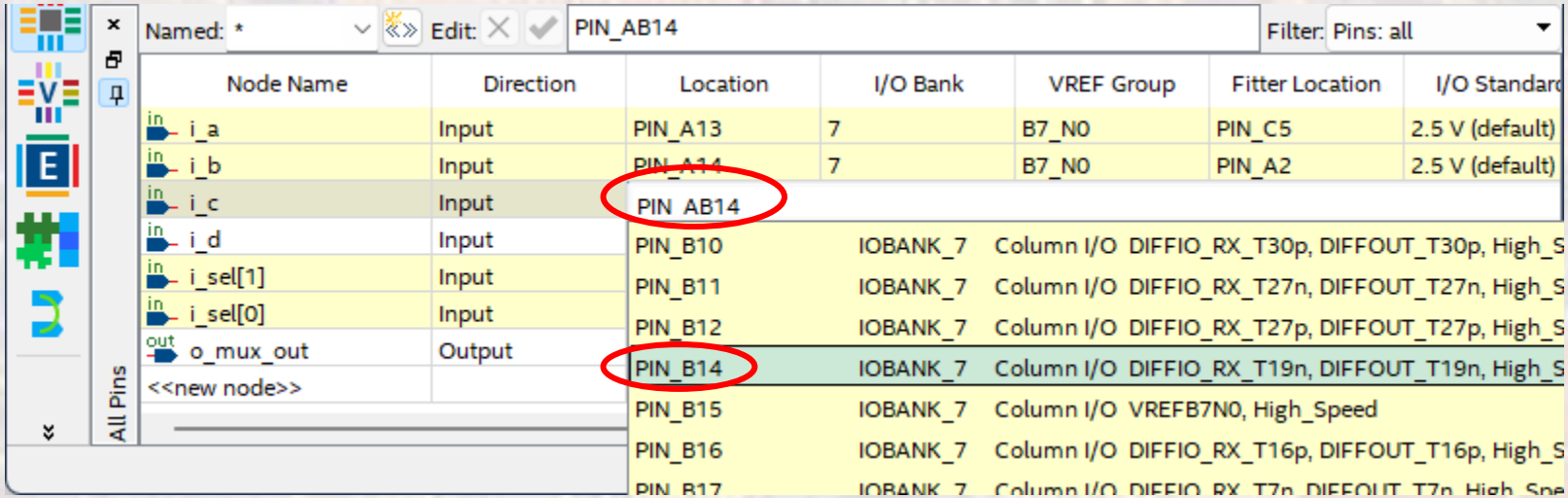
4) Map the schematic pins to DE10 inputs and outputs

- Double click on the location column for a pin
- Select the expand arrow
- Scroll until the desired pin is found and select it
- Close the Pin Planner when finished



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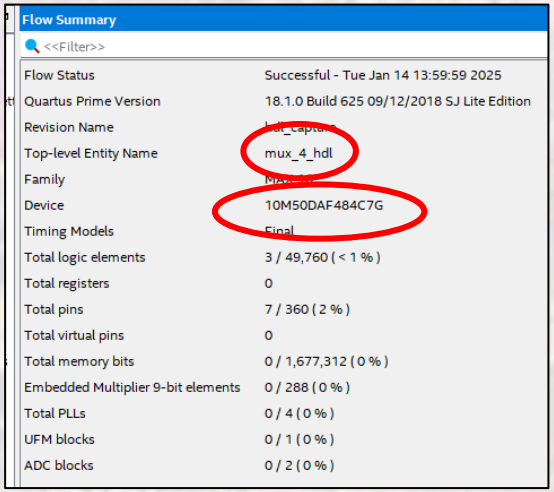
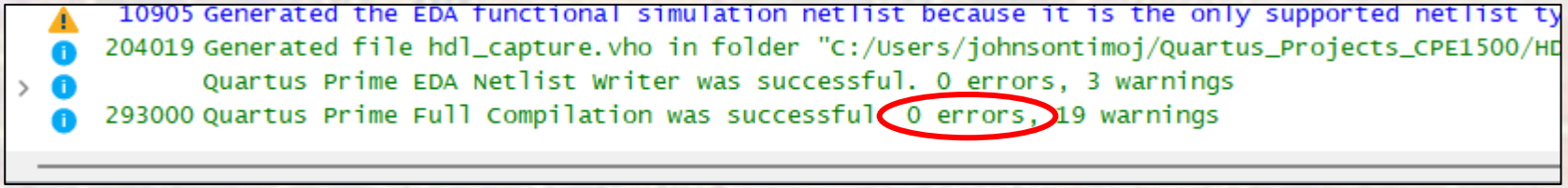
5) Compile the design
   - Save
   - Right click on the design and select Set as Top-Level Entity
   - Processing → Start Compilation
   - Verify success

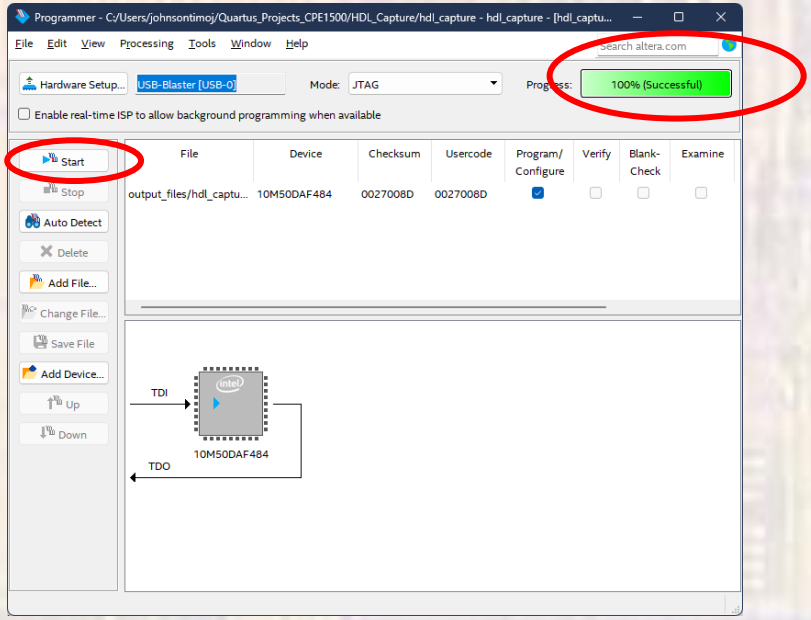




VHDL to DE10

6) Download the design to the DE10

- Plug the DE10 board into your laptop USB port
  - Should be lots of flashing lights
- Tools → Programmer
  - The USB Blaster interface should have been setup when you setup Quartus – see Quartus Setup Slides if it is not visible
- Start



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7) Verify the design
   - Choose a value for SW1 and SW0 (SEL(1) and SEL(0))
   - Verify only the associated SW(9-6) toggle the LED on/off

