CPE 1500 Lab 12: VHDL Registers

1 dedicated lab period, 1 lab period to complete

Objectives

- VHDL design and implementation on the DE10

Prelab **student check off**

- Review the VHDL register and counter slides ☐
- Review the Testbench and DE10 implementation slides ☐

Assignment

Part 1: **Data Register – DE10 implementation**

Use the n-bit data register from the VHDL_Data_Register slides

Use the provided 3Hz clock divider to slow your clock down to a human readable speed

A. Create a DE10 instantiation file with the generic (N) set to 6
   Map 6 switches to the inputs
   Map 6 LEDs to the outputs
   Map the 3Hz clock to an LED

B. Verify the design on the DE10

Part 2: **Design a 4 bit unsigned up/down non-wrapping counter with asynchronous reset.**

Non-wrapping means the counter does not wrap-around to 0 after reaching 15 when counting up and does not wrap-around to 15 after reaching 0 when counting down. In both cases it remains in the terminal state until the direction is changed. UP: 0-1-2-…- 6-7-7-7-7 … DOWN: 7-6-… -1-0-0-0-0 … UP: 0-1-2…

A. Create a testbench and simulate your design

B. Create a DE10 implementation
   Use the provided 3Hz clock divider to slow your clock down to a human readable speed
   Map the count to 4 LEDs
   Map the 3Hz clock to an LED

Check Off

You must demonstrate part 1B and 2B prior to submission of your report

- Demo part 1B results and full part 1 informal report 50%
- Demo part 2B results and full part 2 informal report 50%

Due at 3:00pm on Tuesday following the lab period – in the box

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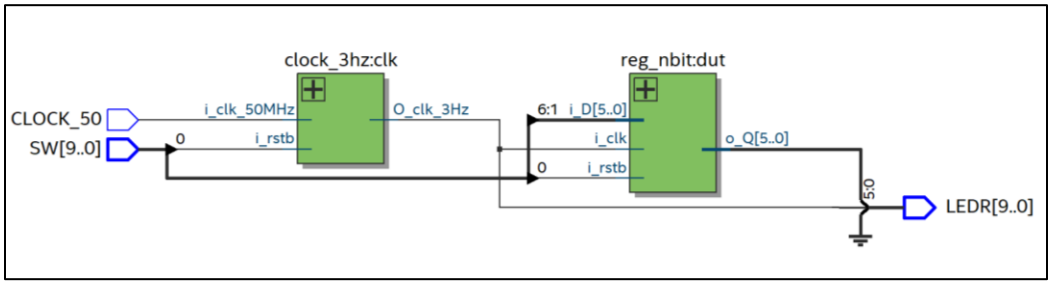
Part 1 RTL



Part 2 RTL