CPE 1500 Lab 3: Integrated Circuits verification

1 dedicated lab period, 1 lab period to complete

Objectives

- Wire up an IC based schematic
- Verify your design (connections)

Prelab

	student check off
• Review the IC Package Technology slides	☐
• Review the IC Package Connection slides	☐
• Review the Design Validation – Proto-Board slides	☐

Assignment

Part 1: **And Gate**

A. Wire up the And gate using the Lab 3 And Gate Schematic

B. Verify the design using the AD2

Use a 2 bit counter signal for the inputs

Print the AD2 results

Verify the results match the And gate expectations

Part 2: **Prime Number Checker**

A. Wire up the Prime Number Checker using the Lab 3 Prime Number Circuit

Use the schematic to map out your connections

B. Verify the design using the AD2

Use a 3 bit binary counter signal for the inputs

Print the AD2 results

Verify the results match the Prime Number Checker expectations

Provide your mapped out connections sheet

Check Off

You must demonstrate parts 1B and 2B prior to submission of your report

- Demo part 1B results and informal report 50%
- Demo part 2B results and informal report 50%

Due at 3:00pm on Tuesday following the lab period – in the box