CPE 1500 Lab 5: VHDL – Logic Design

1 dedicated lab period, 1 lab period to complete

Objectives

- Create simple VHDL logic descriptions
- Simulate and verify in hardware

Prelab

student check off

- N/A ☐

Assignment

Part 1: **Create a logic based VHDL circuit (sum/carry)**

The circuit creates the sum and carry from a 2 input, 1 bit addition

Just like we would do on paper

The circuit will have 3 inputs: a, b, cin

The circuit will have 2 outputs: sum, carry

A. Create a paper description of the design

Create a logic equation for each output

These will be messy – don't try to do any optimization

B. Create a VHDL description of the 1 bit block in Quartus

C. Simulate your design using the University Waveform Viewer

D. Implement your design on the DE10

Use switches for the inputs, use LEDs for the outputs

Part 2: **Create a 4 bit version of your sum/carry circuit**

The circuit creates the sums and carry from a 2 input, 4 bit addition

The design will be structural, using the block from part 1

A. Create a paper block diagram description of the design

B. Create a structural VHDL description in Quartus

C. Simulate your design using the University Waveform Viewer

D. Implement your design on the DE10

Use switches for the inputs, use LEDs for the outputs

Check Off

You must demonstrate parts 1D and 2D prior to submission of your report

- Demo part 1D results and full part 1 informal report 50%
- Demo part 2D results and full part 2 informal report 50%

Due at 3:00pm on Tuesday following the lab period – in the box

Documentation Expectations (appendix)

Paper design

VHDL code

Compilation report

RTL schematic view

Annotated simulation results