Lab 5 Intro

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- Goal:
  - Complete a VHDL design from start to finish
    - Create a logic design from a set of requirements
    - Create VHDL to code the design
    - Run simulations on the VHDL code
    - Synthesize logic and implement it on the DE10
    - Verify the design

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- Process
  - Create a paper solution
  - Review the VHDL Generation slides
  - Create VHDL code for your design
  - Review the VHDL Simulation via University Waveform Viewer slides
  - Run a simulation of your design
    - Determine the inputs
    - Verify the outputs
  - Review the VHDL to DE10 slides
  - Implement your design on the DE10
    - Synthesize
    - Map Pins
    - Program
  - Verify the design
- Repeat for Part 2