CPE 1500 Lab 7: Logic Reduction and Synthesis

1 dedicated lab period, 1 lab period to complete

Objectives

- Practice logic reduction techniques
- Synthesize designs based on equation inputs

Prelab

student check off

- N/A ☐

Assignment

Part 1: **Logic Reduction – Boolean Laws**

Reduce the following logic equation to SOP form using the Boolean Laws

A'(B + C')(A + D)

A. Create a Quartus schematic for your design
B. Simulate your design using the University Waveform Viewer
C. Implement your design on the DE10
   Use switches for the inputs, use LEDs for the outputs

Part 2: **Logic Reduction - Kmaps**

Reduce the following logic equation to POS form using Kmaps

A'(B + C')(A + D)

A. Create a complete truth table from the equation
B. Create a paper schematic for your reduced (POS) solution
C. Implement your design on the breadboard using parts from the kit or the tech center
D. Create a measured truth table for the design
   Use the AD2 to test your design

Part 3: **Logic Synthesis - Multiplexer**

Implement the following logic equation using a multiplexor

A'(B + C') + AB'

A. Create a complete truth table from the equation
B. Map the truth table to the inputs of the 74LS151 multiplexor
C. Implement your design on the breadboard
D. Create a measured truth table for the design
   Use the AD2 to test your design

Check Off

You must demonstrate part 2D prior to submission of your report

- Full part 1 informal report 35%
- Demo part 2D results and full part 2 informal report 35%
- Full part 3 informal report 30%

Due at 3:00pm on Tuesday following the lab period – in the box