CPE 1500 Lab 8: VHDL Logic Synthesis

1 dedicated lab period, 1 lab period to complete

Objectives

- Synthesize logic blocks using VHDL

Prelab

student check off

- Review the HEX (seven segment) display notes ☐

Assignment

Part 1: **2 output multiplexer**

Create an 8 input multiplexer with one set of data inputs, 2 sets of select inputs and 2 data outputs

A. Create a hand drawn top level block diagram
B. Write VHDL code to behaviorally model your design
C. Simulate your design using the University Waveform Viewer

Part 2: **Logical Shift Left/Right by 2 block**

Create a 6 bit shifter that can do a logical shift left or right by 2

A. Create a hand drawn top level block diagram
B. Write VHDL code to behaviorally model your design
C. Simulate your design using the University Waveform Viewer

Part 3: **Hex to Seven Segment decoder**

Create a 4bit input → seven segment display decoder for Hex numbers

A. Create a hex to seven segment decoder block
B. Simulate your hrx to seven segment decoder block
C. Instantiate 2 of these blocks into a DE10 top level design
   Map your inputs to 2 sets of 4 switches
   Map your output to 2 of the HEX (sseg) displays

Check Off

You must demonstrate part 3C prior to submission of your report

- Full part 1 informal report 30%
- Full part 2 informal report 30%
- Demo part 3C results and full part 3 informal report 40%

Due at 3:00pm on Tuesday following the lab period – in the box