CPE 1500 Lab 9: VHDL Logic Synthesis - SSEG

1 dedicated lab period, 1 lab period to complete

Objectives

- Synthesize logic blocks using VHDL

Prelab

student check off

- Review the HEX (seven segment) display notes ☐

Assignment

Part 1: **Hex to Seven Segment decoder**

Create a 4bit input → seven segment display decoder for Hex numbers

A. Create a hex to seven segment decoder block

B. Simulate your hex to seven segment decoder block

C. Instantiate 2 of these blocks into a DE10 top level design

Map your inputs to 2 sets of 4 switches

Map your output to 2 of the HEX (sseg) displays

Check Off

You must demonstrate part 1C prior to submission of your report

- Demo part 1C results and full part 1 informal report 100%

Due at 3:00pm on Tuesday following the lab period – in the box