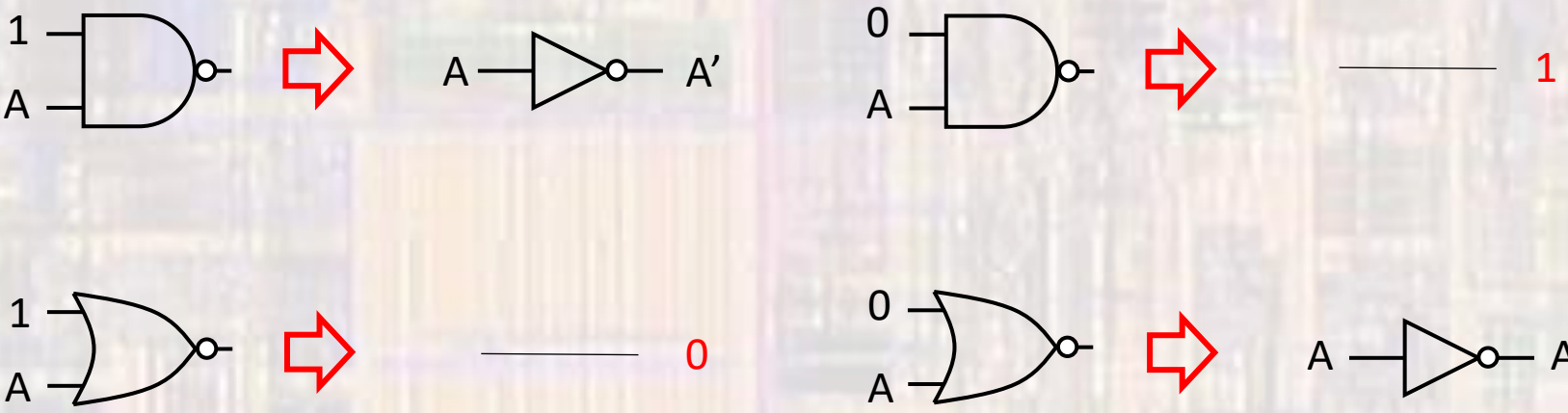
Latches

Last updated 11/12/24

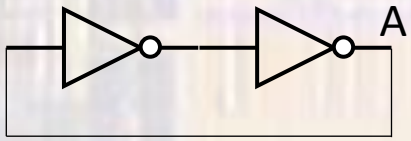
Latches

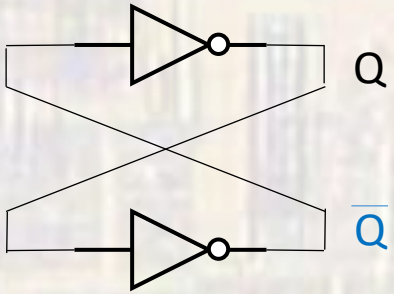
- Shortcuts



Latches

- Bi-stable circuit
  - Sequential Circuit ?
  - Circuit with 2 stable operating points
  - Holds 1 element of memory
    - 1 state variable
    - 2 values for the state variable
      - 1 bit – 0 or 1





state variable

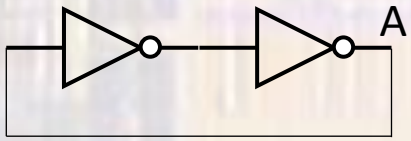
State	A
0	0
1	1

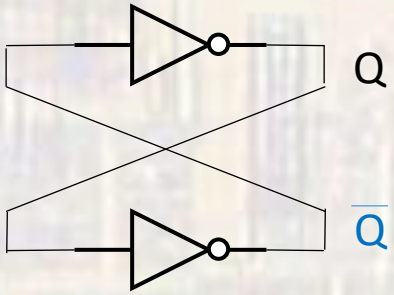
state variable

State	Q	$\overline{Q}$
0	0	1
1	1	0

Latches

- Bi-stable circuit
  - Sequential Circuit ?
  - Circuit with 2 stable operating points
  - Holds 1 element of memory
    - 1 state variable
    - 2 values for the state variable
      - 1 bit – 0 or 1





What's wrong with this circuit

state variable

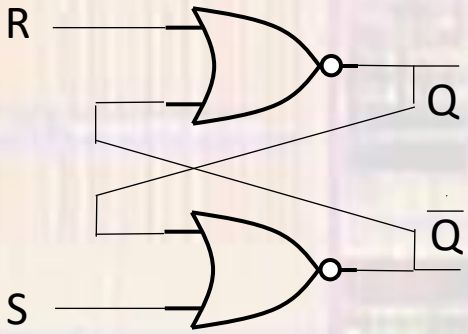
State	A
0	0
1	1

state variable

State	Q	$\overline{Q}$
0	0	1
1	1	0

Latches

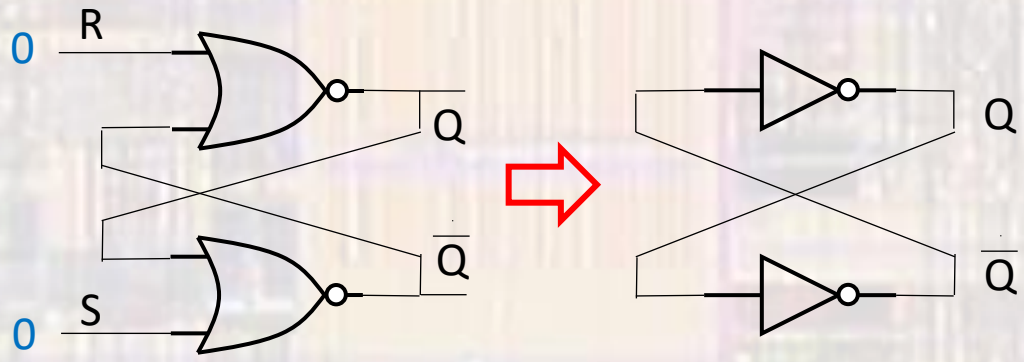
- SR Latch (set/reset)
  - Asynchronous Sequential Circuit
    - Sequential - Output depends on Inputs and 1 state variable Q (Q_{old})
    - Asynchronous – output changes occur when inputs change
    - Memory is in the bi-stable latch



R : Reset
S : Set

Latches

- SR Latch (set/reset)
  - 0,0 Inputs

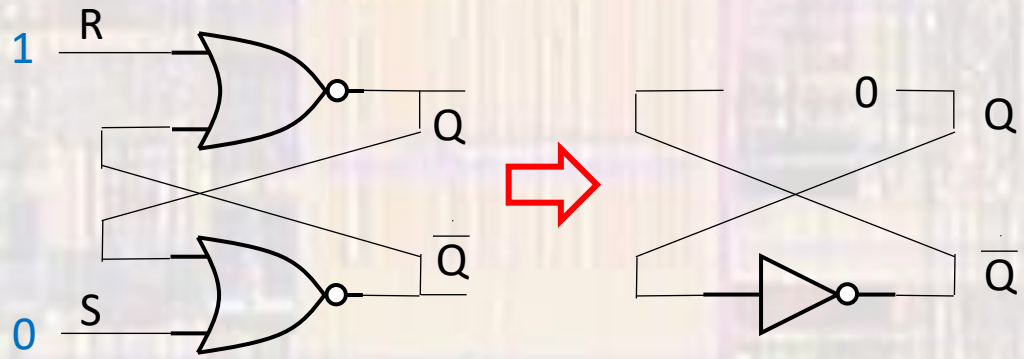


Latch

S	R	Q
0	0	Q_{old}

Latches

- SR Latch (set/reset)
  - 0,1 Inputs

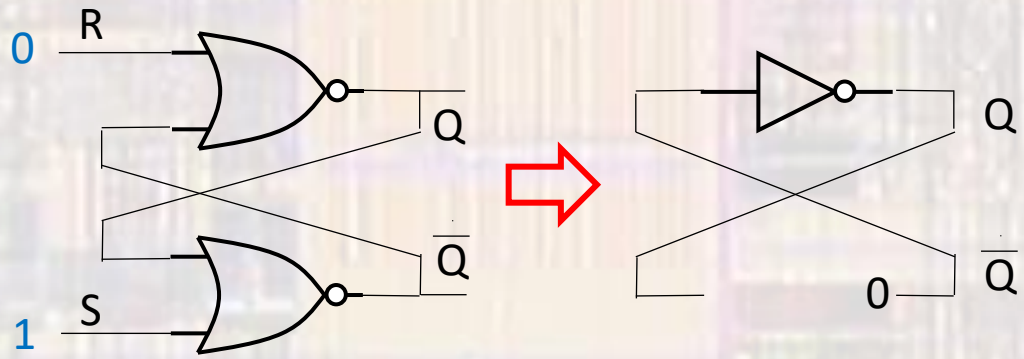


S	R	Q
0	0	Q_{old}
0	1	0

Reset

Latches

- SR Latch (set/reset)
  - 1,0 Inputs

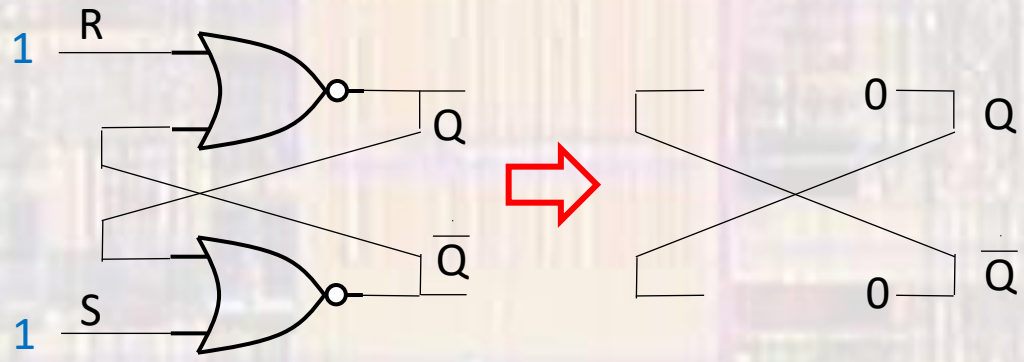


Set

S	R	Q
0	0	Q_{old}
0	1	0
1	0	1

Latches

- SR Latch (set/reset)
  - 1,1 Inputs

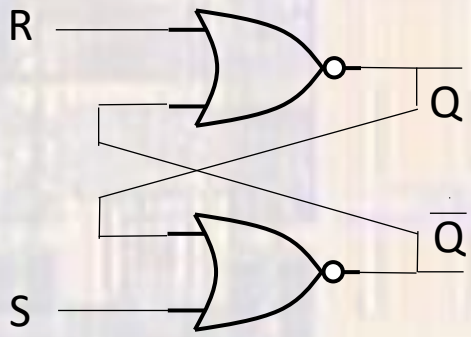


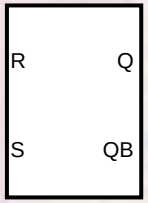
S	R	Q
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

Fault?

Latches

- SR Latch (set/reset)

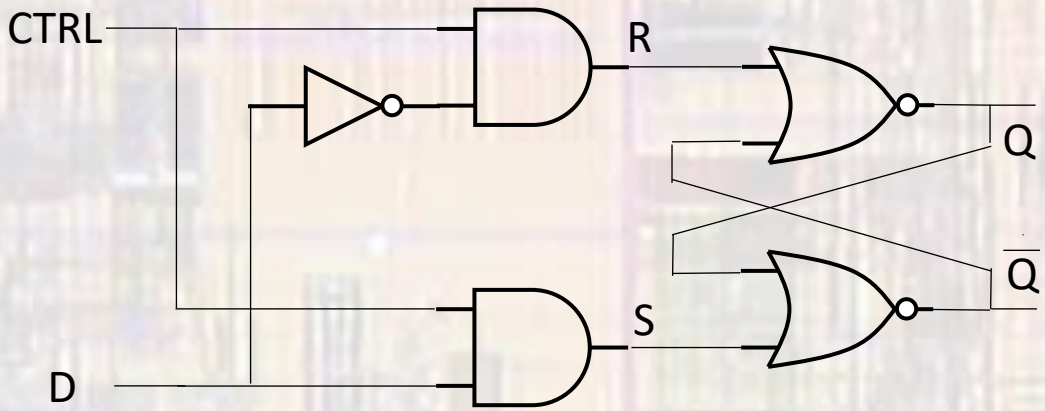




S	R	Q
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

Latches

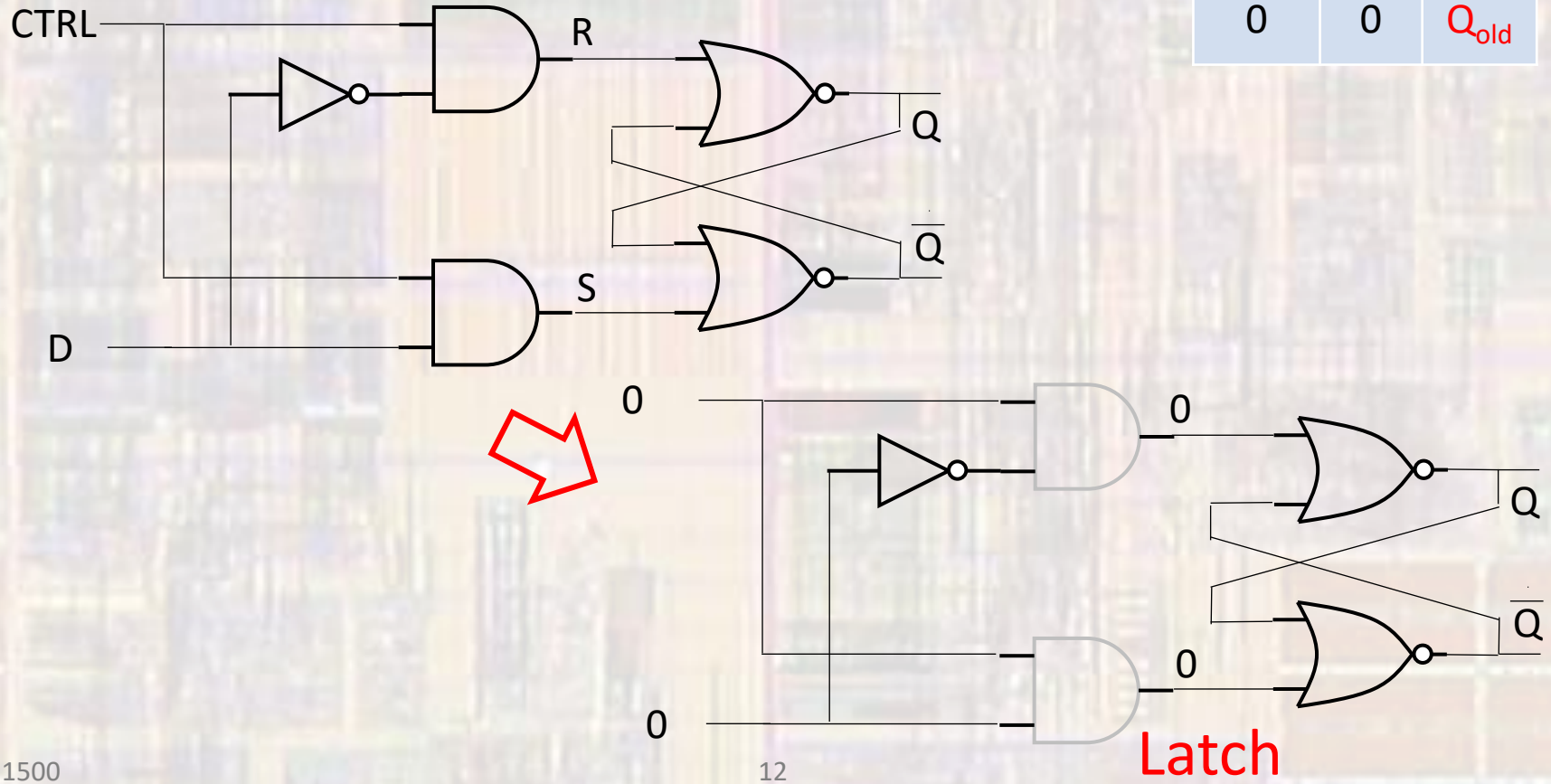
- D Latch (data)
  - Asynchronous Sequential Circuit
    - Sequential - Output depends on Inputs and 1 state variable Q (Q_{old})
    - Asynchronous – output changes occur when inputs change
    - Memory is in the bi-stable latch



Latches

- D Latch (data)
  - 0,0 inputs – control (CTRL), data (D)

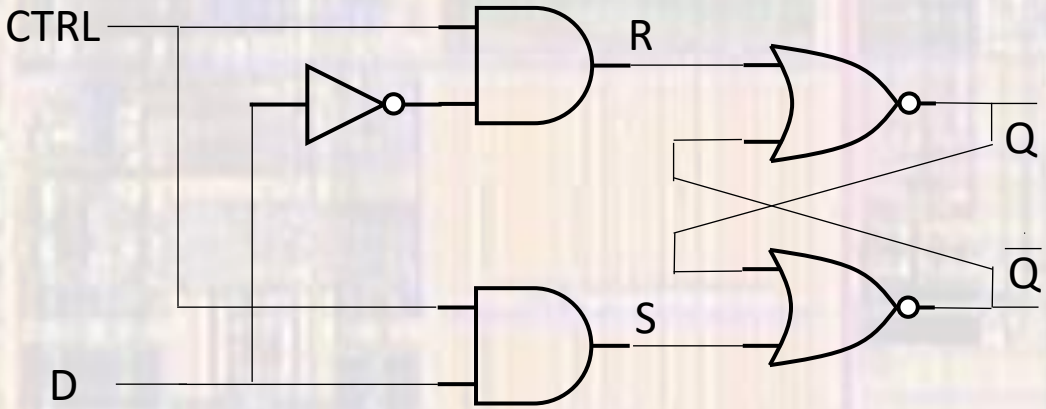
CTRL	D	Q
0	0	Q_{old}

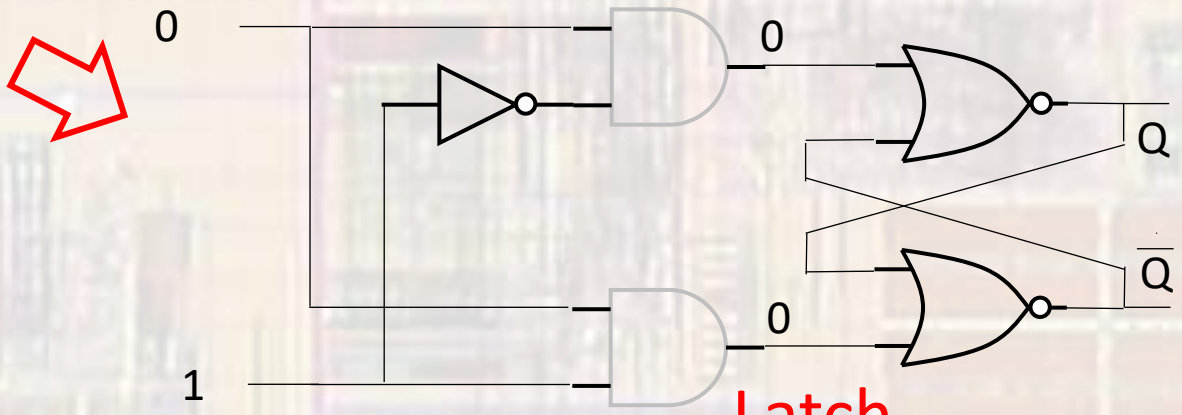


Latches

- D Latch (data)
  - 0,1 inputs – control, data

CTRL	D	Q
0	0	Q_{old}
0	1	Q_{old}

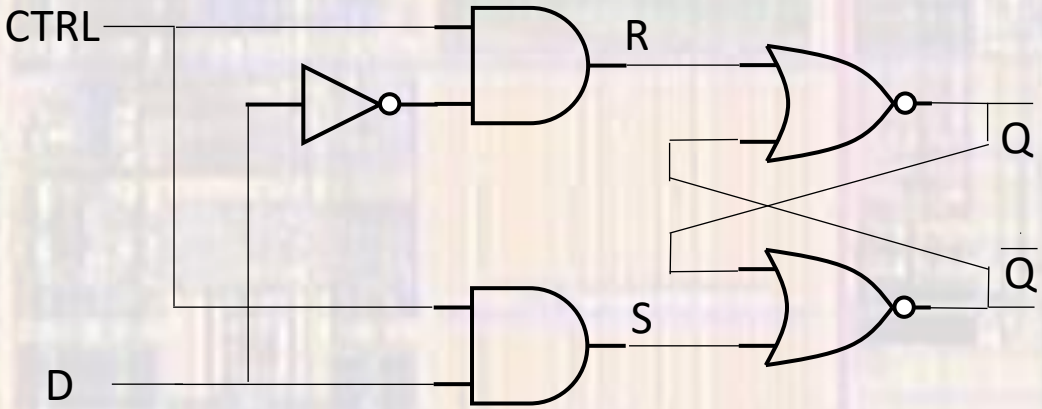




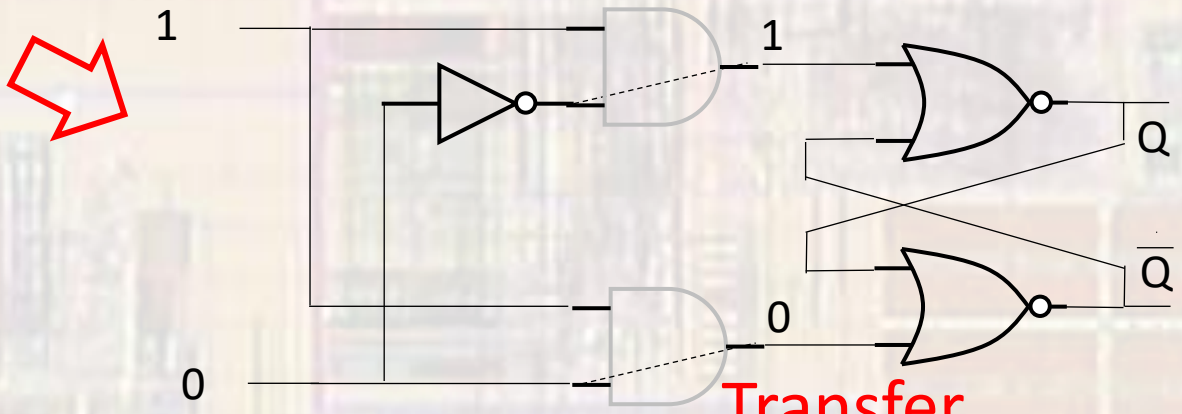
Latch

Latches

- D Latch (data)
  - 1,0 inputs – control, data



CTRL	D	Q
0	0	Q_{old}
0	1	Q_{old}
1	0	0 (D)

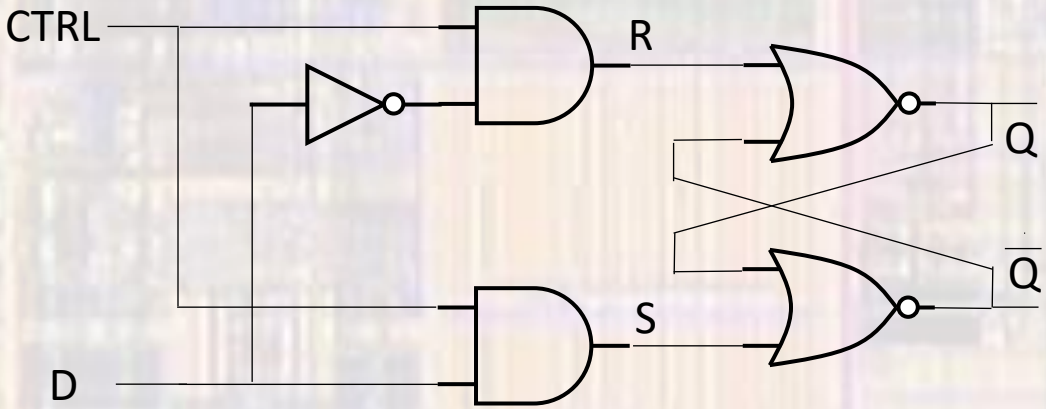


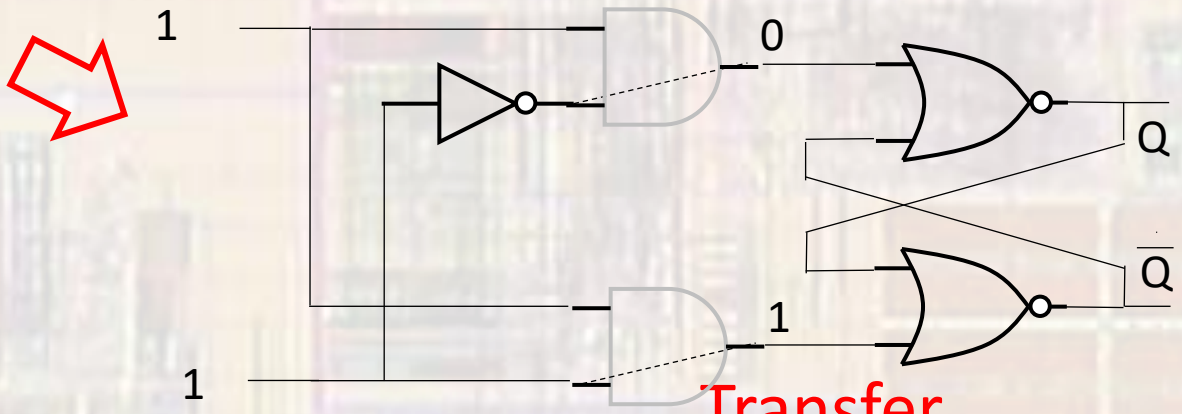
Transfer

Latches

- D Latch (data)
  - 1,1 inputs – control, data

CTRL	D	Q
0	0	Q_{old}
0	1	Q_{old}
1	0	0 (D)
1	1	1 (D)





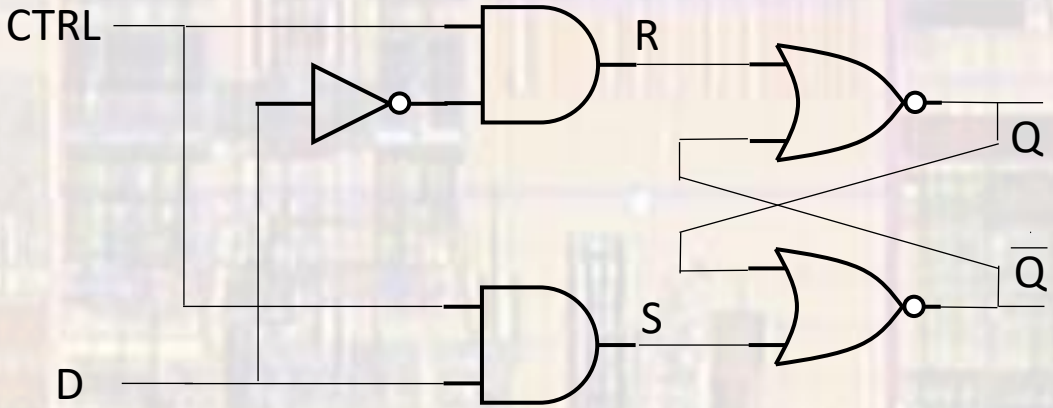
Transfer

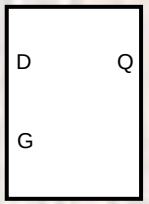
Latches

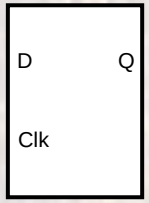
- D Latch (data)

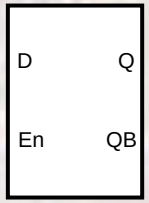
Level Sensitive Latch

CTRL = low → latched
CTRL = high → Transfer





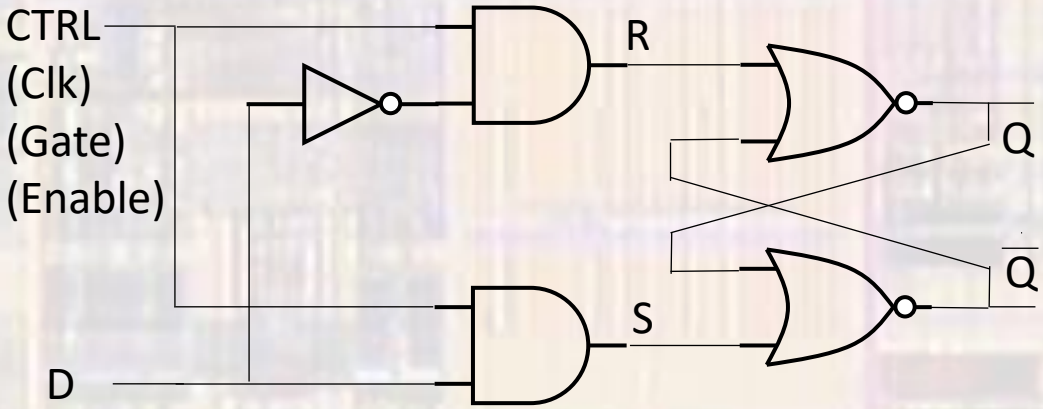


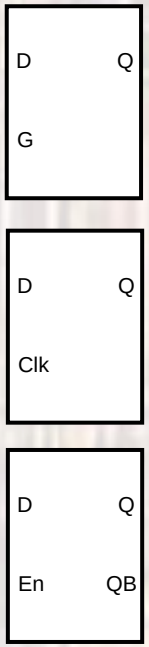


CTRL	D	Q
0	x	Q_{old}
1	D	D

Latches

- D Latch (data)
  - Control input: Clk(clock), G (gate), En (enable)

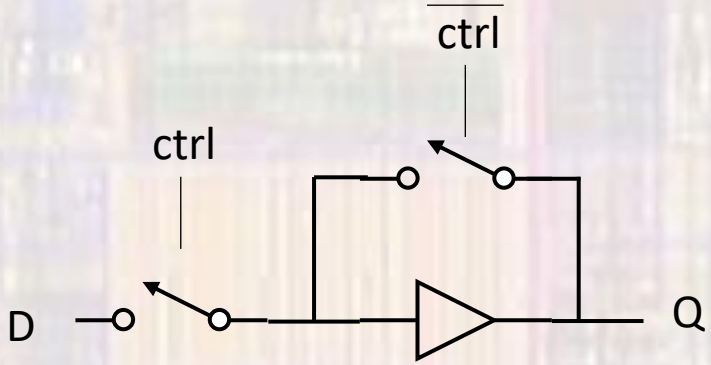




CTRL	D	Q
0	x	Q_{old}
1	D	D

Latches

- D Latch - Abstraction



CTRL	D	Q
0	x	Q_{old}
1	D	D