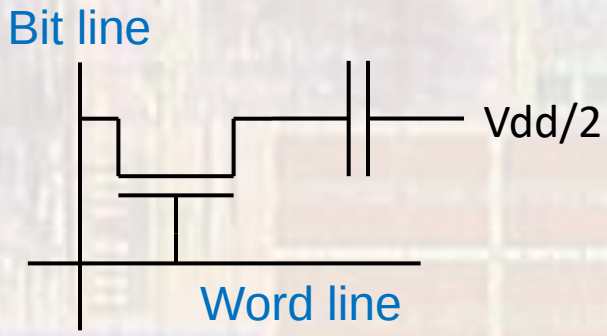
SDRAM

Last updated 3/26/25

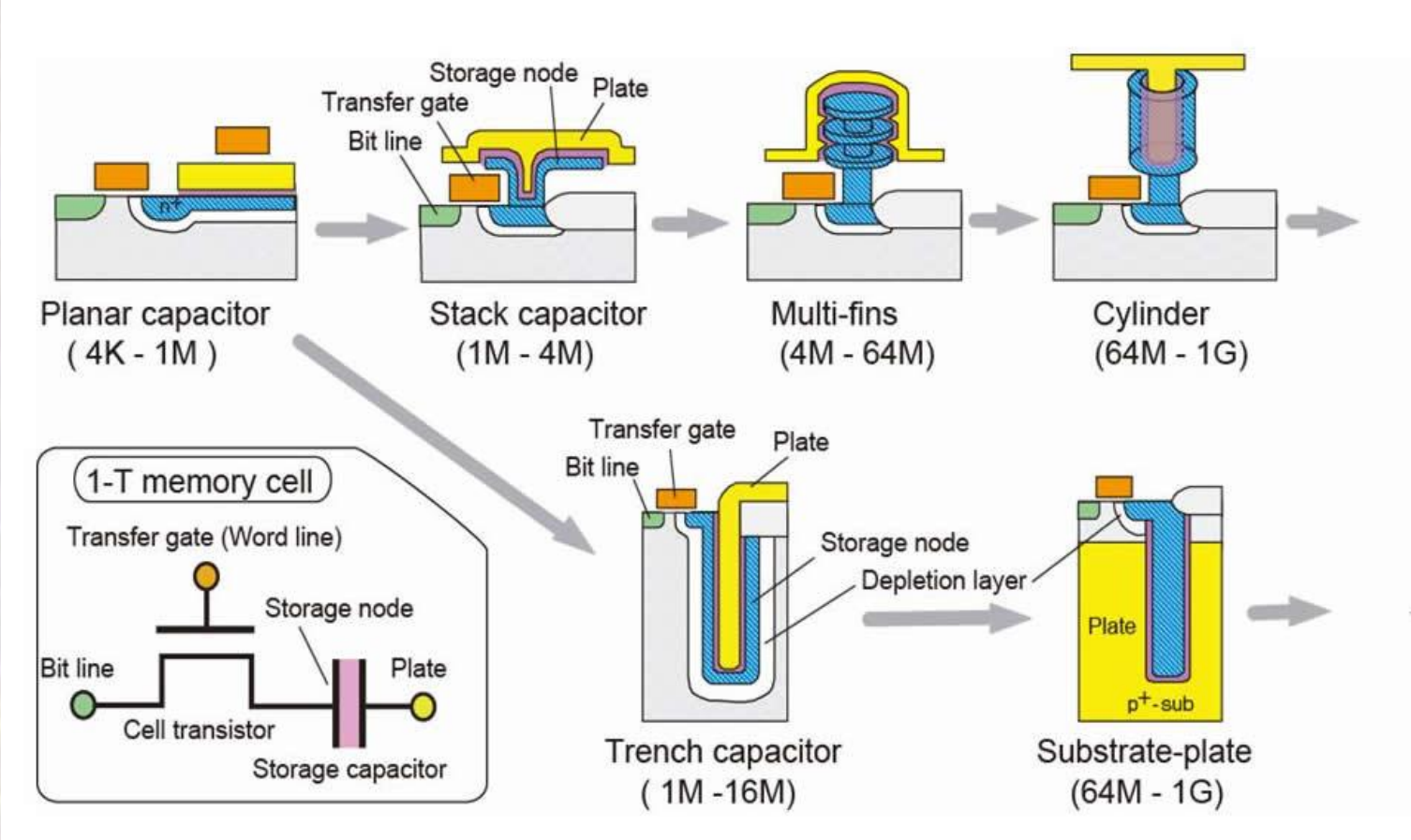
Memory - SDRAM

- SDRAM – Synchronous Dynamic Random Access Memory
  - Memory cell (1 bit) is based on capacitor charge storage
  - Bit value decays over time
    - must be recharged – called a refresh cycle
  - Standard SDRAM transfers 1 word each array access
    - DDR – double data rate – transfers 2 words each array access
    - DDR2, DDR3, DDR4 – transfer 4,8,16 words each array access
  - Medium speed
  - Highest density
  - Used as main memory



Memory - SDRAM

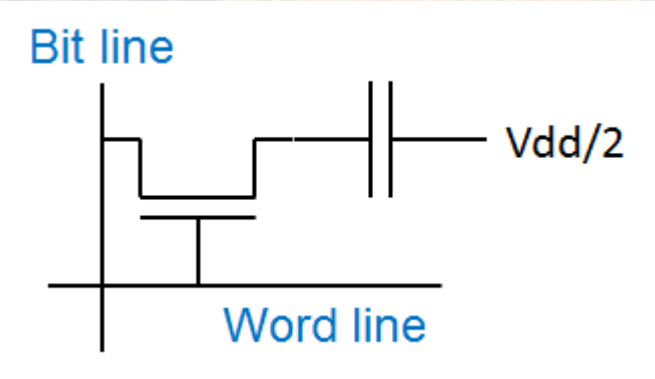
- SDRAM – Cell

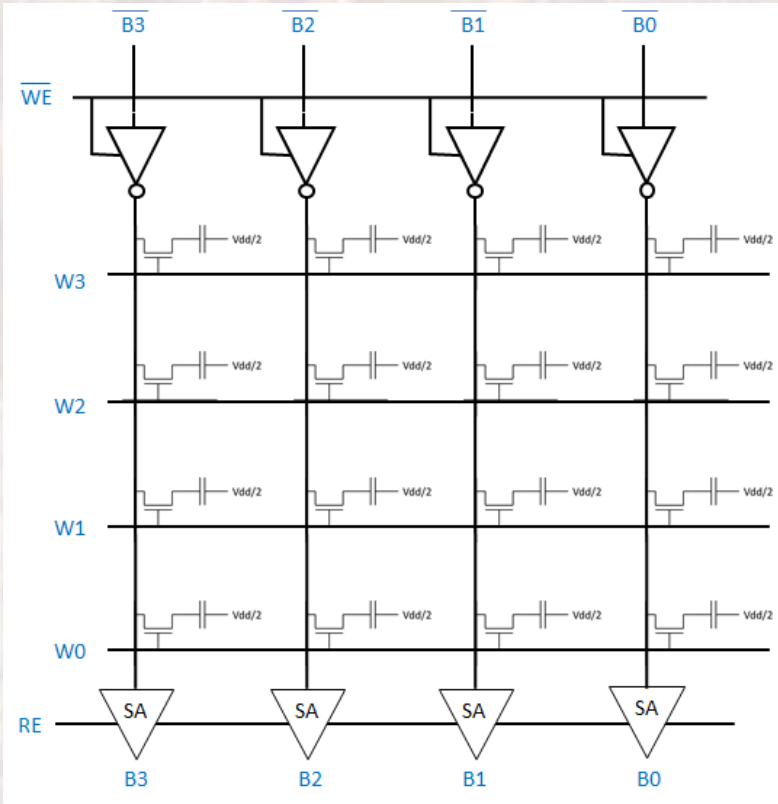


Src: IEDM

Memory - SDRAM

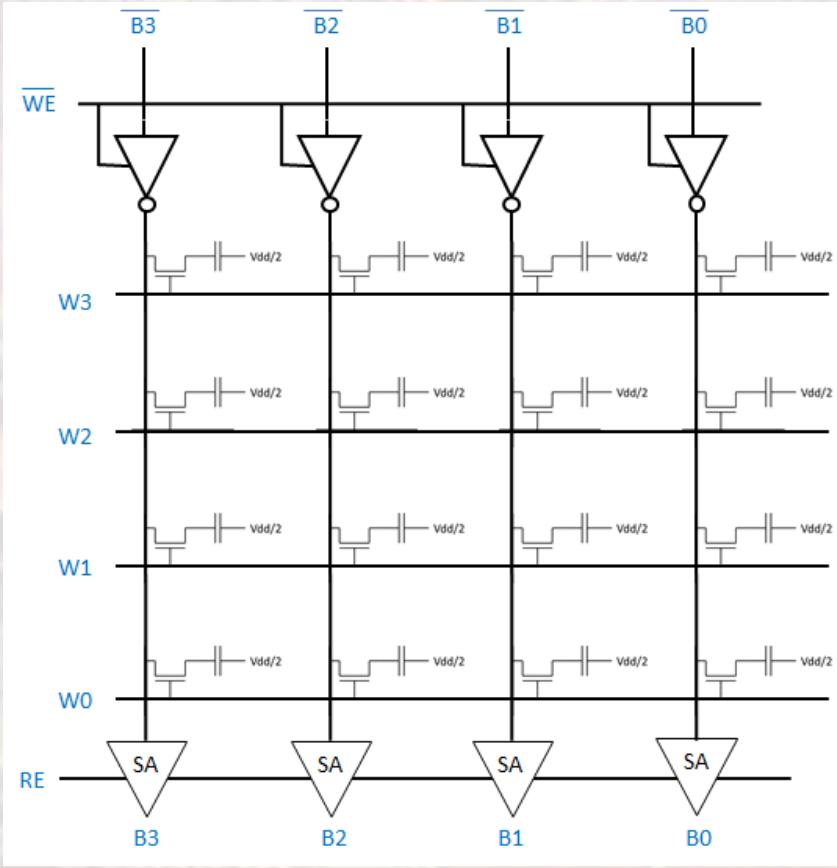
- SDRAM – Synchronous Dynamic Random Access Memory
  - Write
    - All Word lines low
    - Read Enable (RE) disabled (low)
    - Place $\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ on inputs
    - Pull write enable bar ($\overline{WE}$) low
    - Strobe the desired word line high
    - Bit lines write to the bit cell capacitors





Memory - SDRAM

- SDRAM – Synchronous Dynamic Random Access Memory
  - Read
    - All Word lines low
    - Write enable bar ($\overline{WE}$) high
      - inverters tristated
    - Read Enable (RE) high
    - Strobe the desired word line high
    - Sense amplifiers read the value of the capacitors
    - The read process is destructive !
      - WHY?



Memory - SDRAM

- SDRAM – Dynamics
  - C_{cell} ~ 1/10 $C_{bitline}$
  - Charge redistribution → small voltage changes
  - Cell charge = Q_{cell} = +/- (Vdd/2 * C_{cell})
  - Bitline charge = $Q_{bitline}$ = Vdd/2 * $C_{bitline}$
    - Assuming $V_{bitline}$ precharged to Vdd/2
  - $\Delta V = \frac{V_{dd}}{2} \times \left(\frac{C_{cell}}{C_{cell}+C_{bitline}}\right) = 0.045V_{dd} = 122\text{mV} \text{ @ } 2.7\text{V}$