Multiplexors

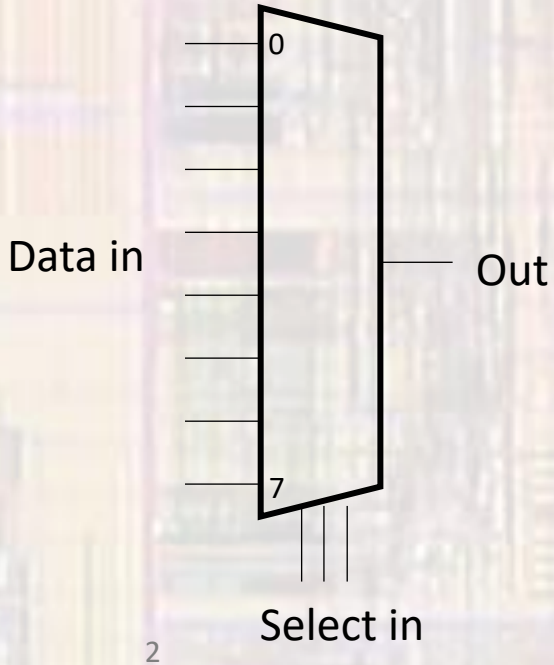
Last updated 10/30/24

Multiplexors

- A multiplexor selects one of many inputs and routes it to the output
  - N data inputs – typically a power of 2
    - N:1 Multiplexor
  - S control (select) inputs – $\log_2(N)$
  - 1 output

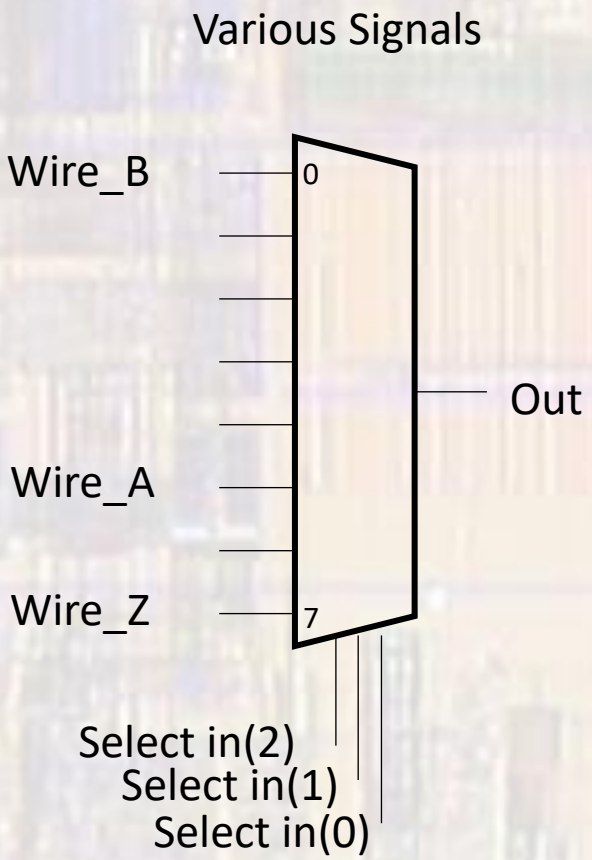
N = 8

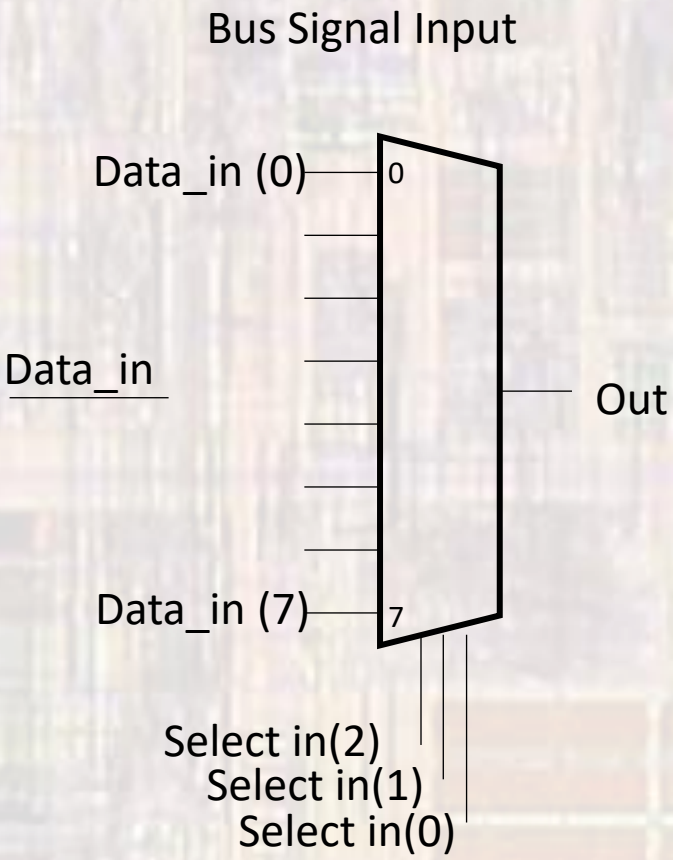
S = 3



Multiplexors

- A closer look



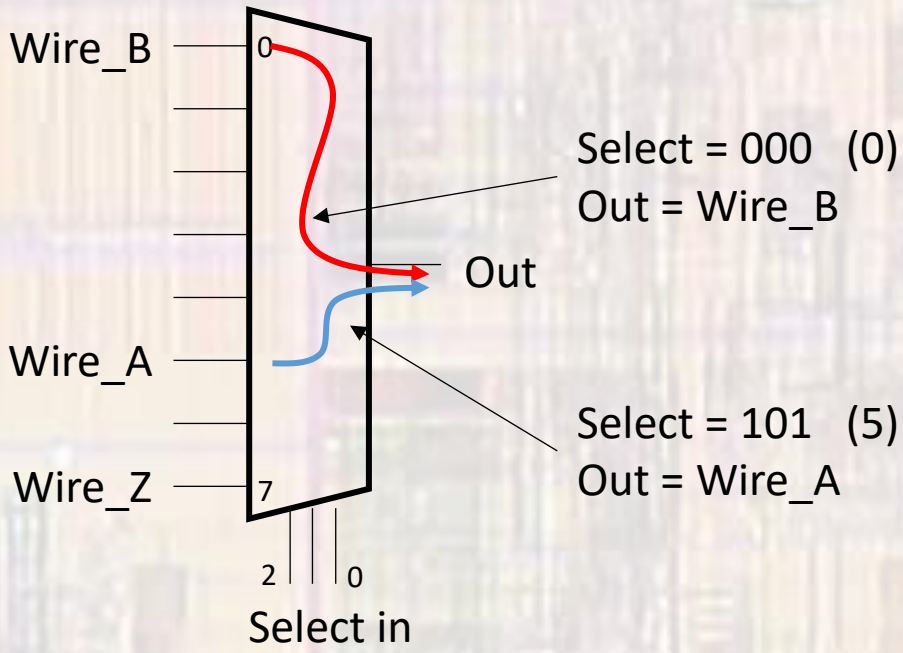


Multiplexors

- Select process
  - Connect the input associated with the binary value of the select signal to the output

N = 8

S = 3



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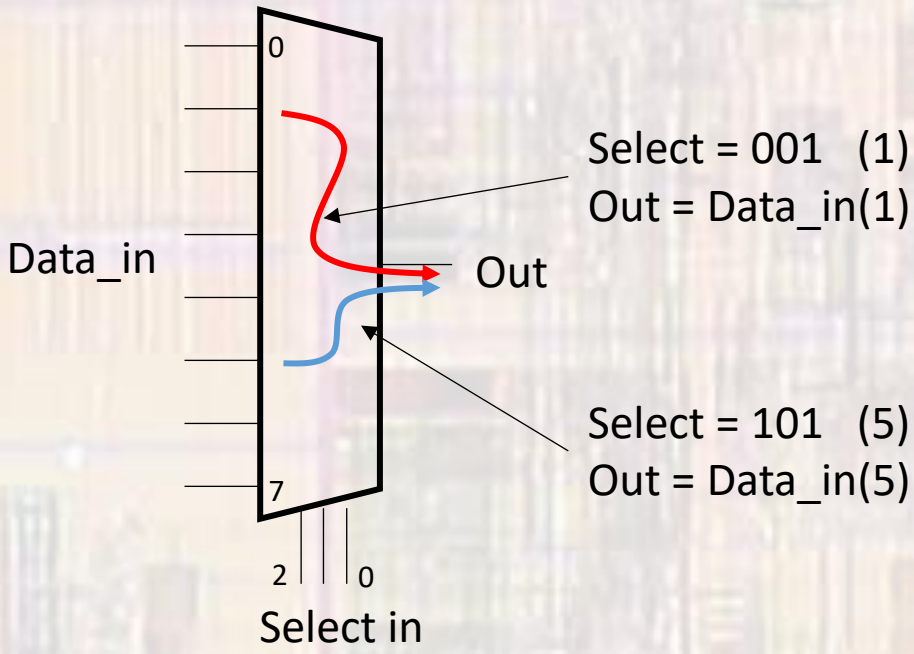
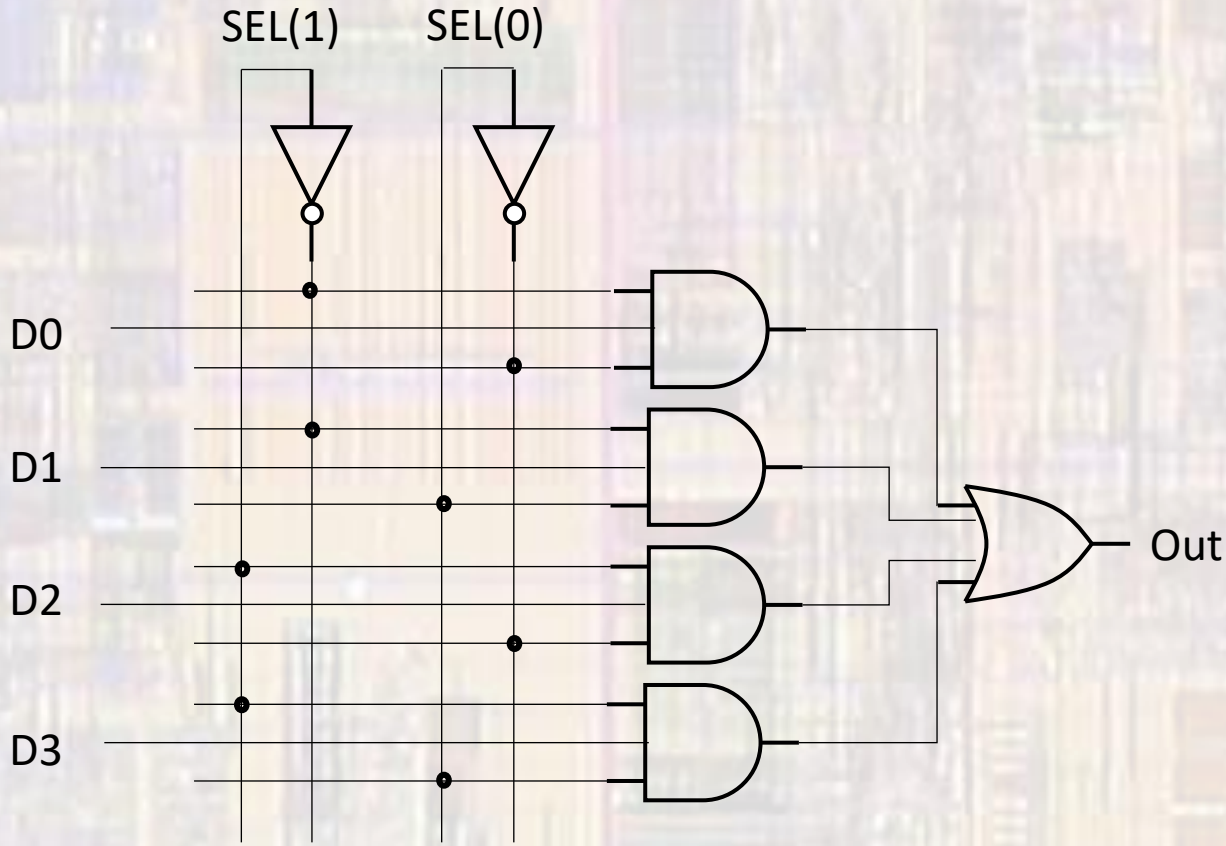


Multiplexors

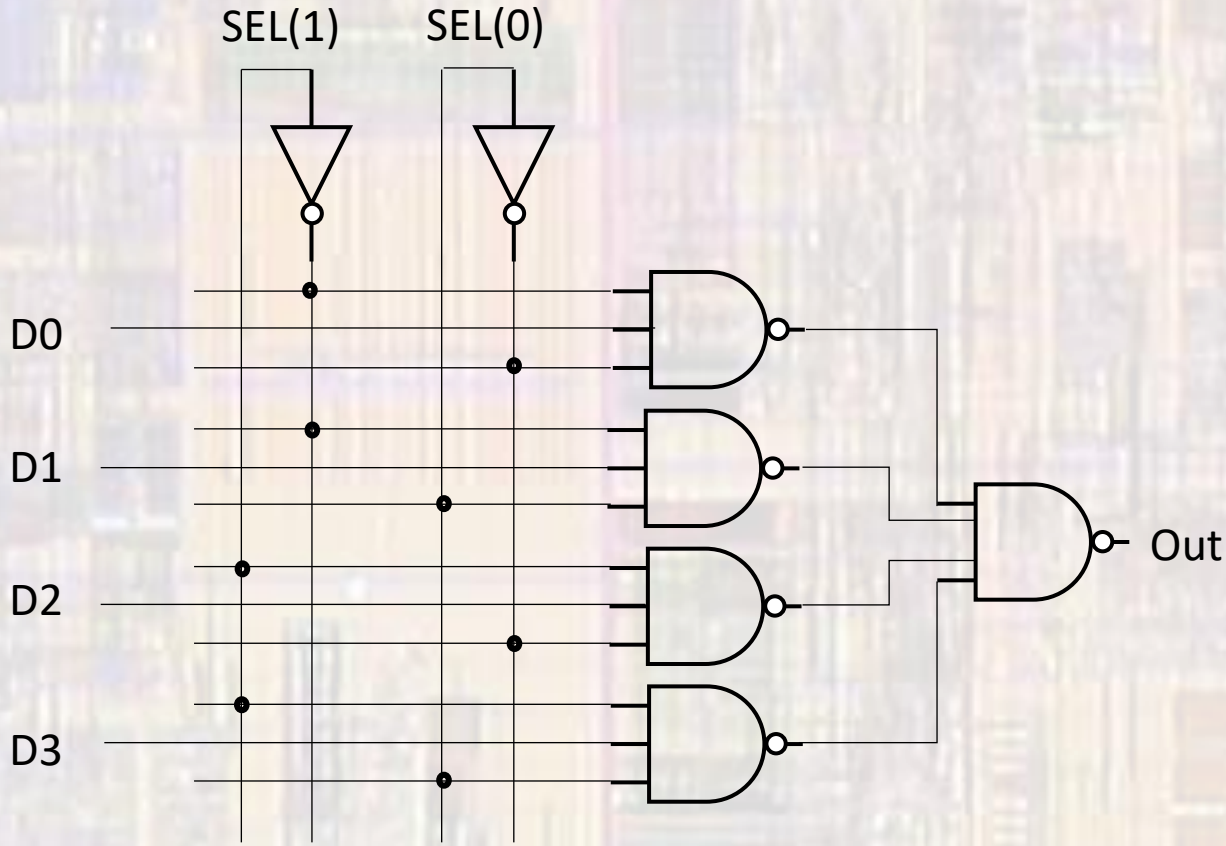
- Implementation - 1
  - Direct Synthesis

$$Out = \overline{S1}\ \overline{S0}\ D0 + \overline{S1}\ S0\ D1 + S1\ \overline{S0}\ D2 + S1\ S0\ D3$$



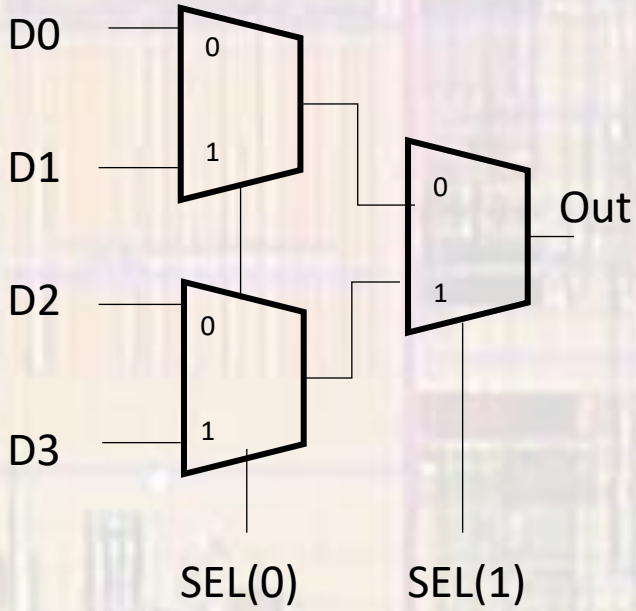
Multiplexors

- Implementation - 2
  - Optimized



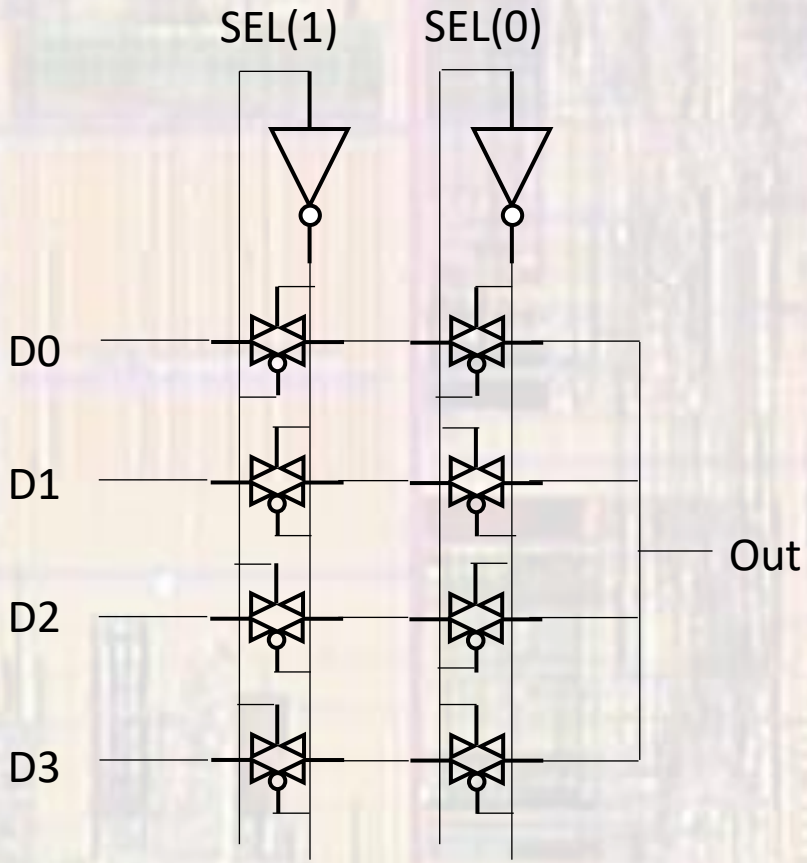
Multiplexors

- Implementation - 3
  - Multi-level Mux



Multiplexors

- Implementation - 4
  - Pass-Gate (Transmission gate)



Smallest solution

Why might this not be a good solution