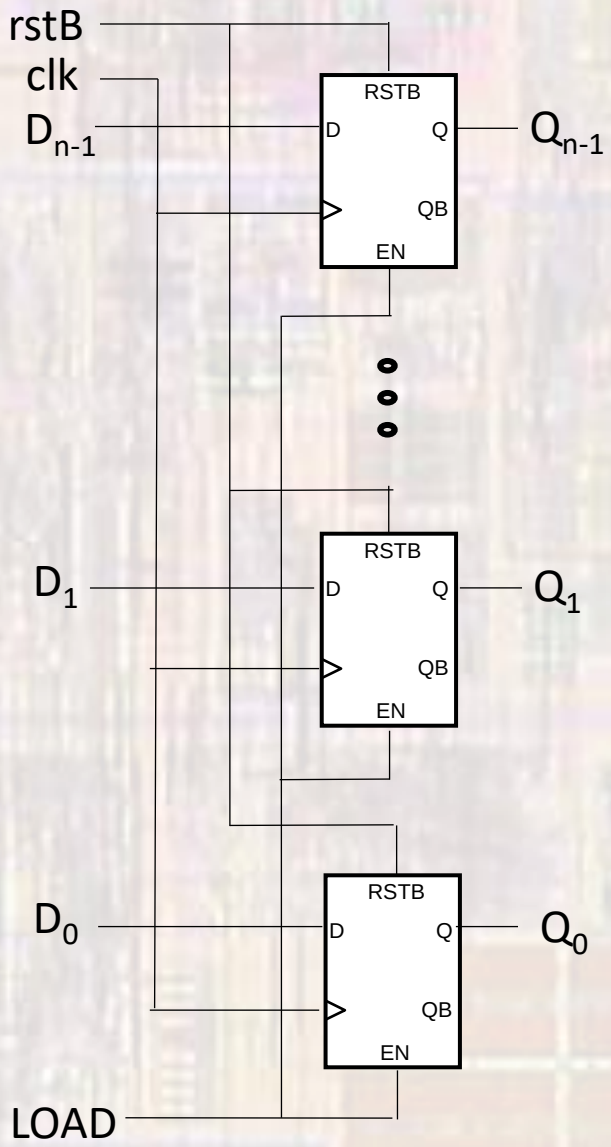
Registers

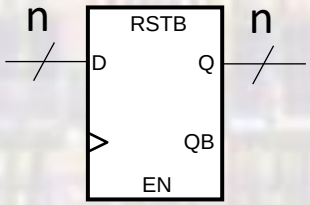
Last updated 1/9/25

Registers

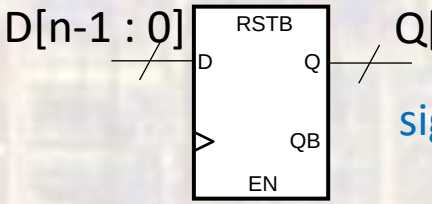
- Data Register
  - Collection of n Flip-Flops
  - Configured in parallel
  - Common clock, set/reset, enable
  - Stores an n-bit state variable



n-bit register



n bit wide bus



signal indices n-1 down to 0

Registers

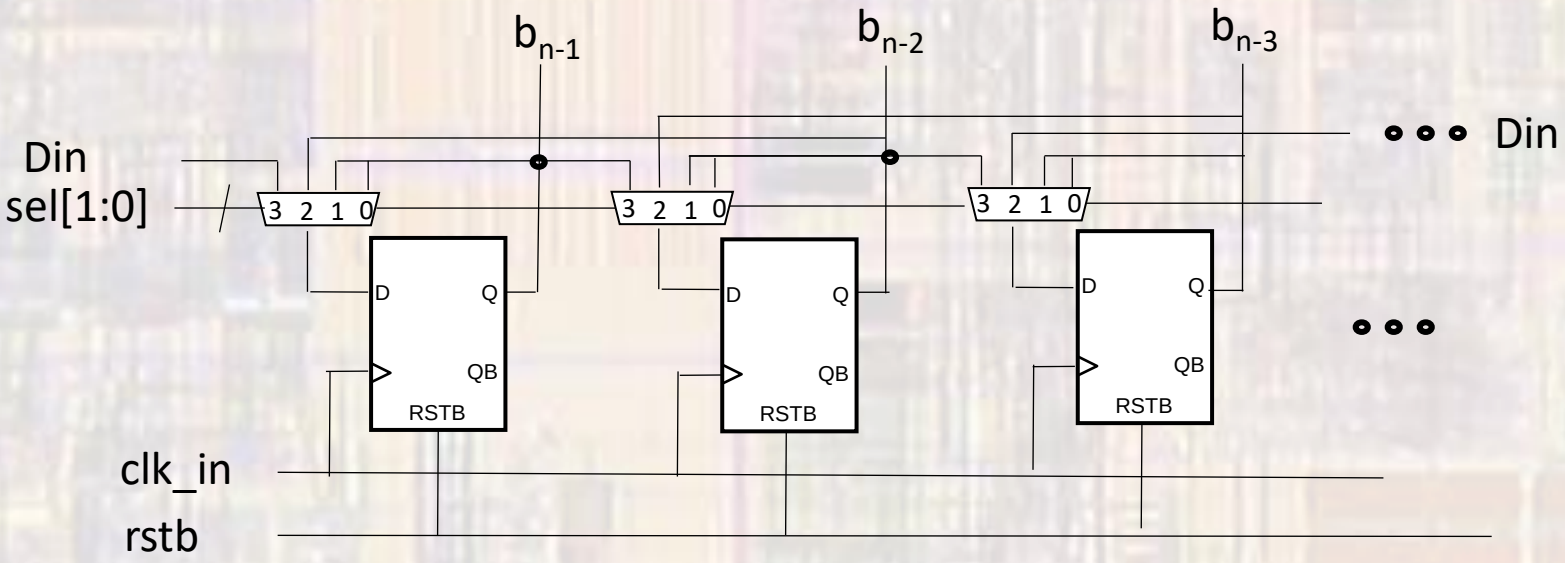
- Shift Register
  - Shift a series of bits within a register
  - Left/right
  - N bit shift
  - Wrapping (rotate)
    - Load register with load signal
    - Direction
  - Non-wrapping
    - Data input – both sides
    - Direction

DATA	dir	load	Din	result
XXXXX	X	1	00100	00101
00101	R	0	XXXXX	10010
00101	L	0	XXXXX	01010

Din	DATA	dir	result
1	00100	R	10010
0	10010	R	01001
1	01001	L	10011

Registers

- Shift Register
  - Non-wrapping, Data in (from both ends)
    - sel[0]: dir : right(1) / left(0)
    - sel[1]: shift: shift(1) / no-shift(0)



Registers

- Rotate Register
  - Wrapping, needs a load signal
    - SEL: 0 0 load
    - SEL: 0 1 Idle
    - SEL: 1 0 Shift left
    - SEL: 1 1 Shift right