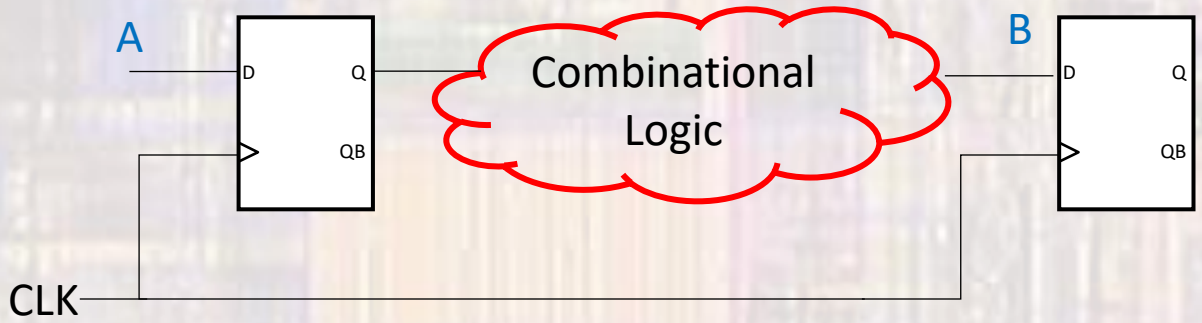
RTL Timing Analysis

Last updated 12/12/24

RTL Timing Analysis

- Typical Flip-Flop Circuit



- Need the data to get from point A to point B before the next clock edge occurs

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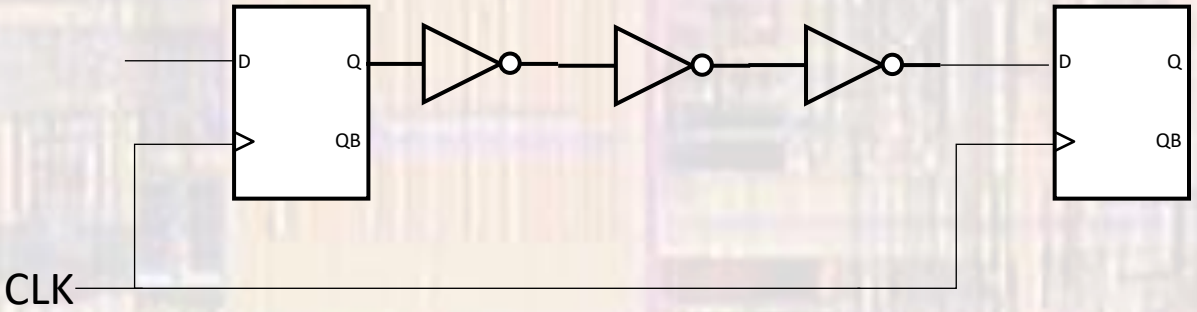
RTL Timing Analysis

- Flip-Flop Example
  - t_{PD} INV = 10ps
  - t_{CQ} = 22ps
  - t_{setup} = 4ps
  - t_{hold} = 2ps

All values already account for loading



Shortest clock period = $t_{CQ} + t_{INV} + t_{INV} + t_{INV} + t_{setup}$ = 56ps
Fastest clock speed = 17.857GHz

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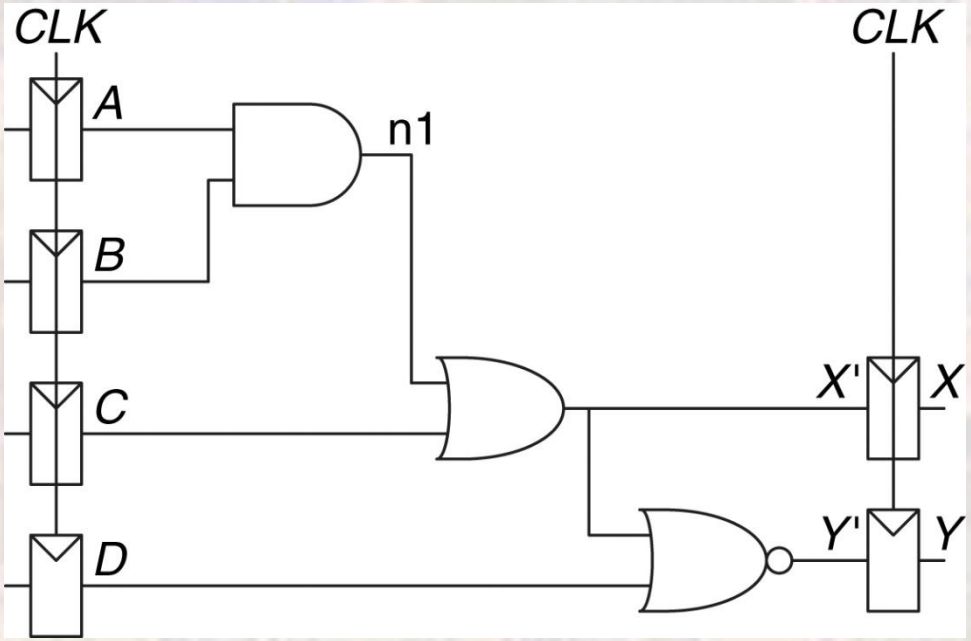
RTL Timing Analysis

- RTL Example

All values already account for loading



src: Harris & Harris

t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

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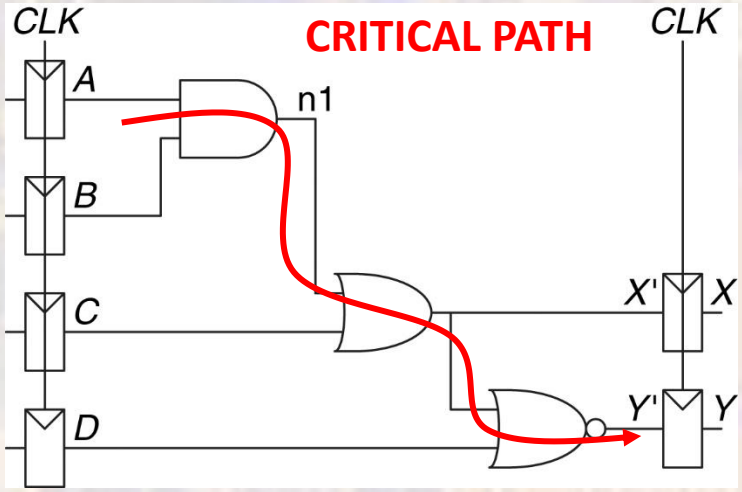
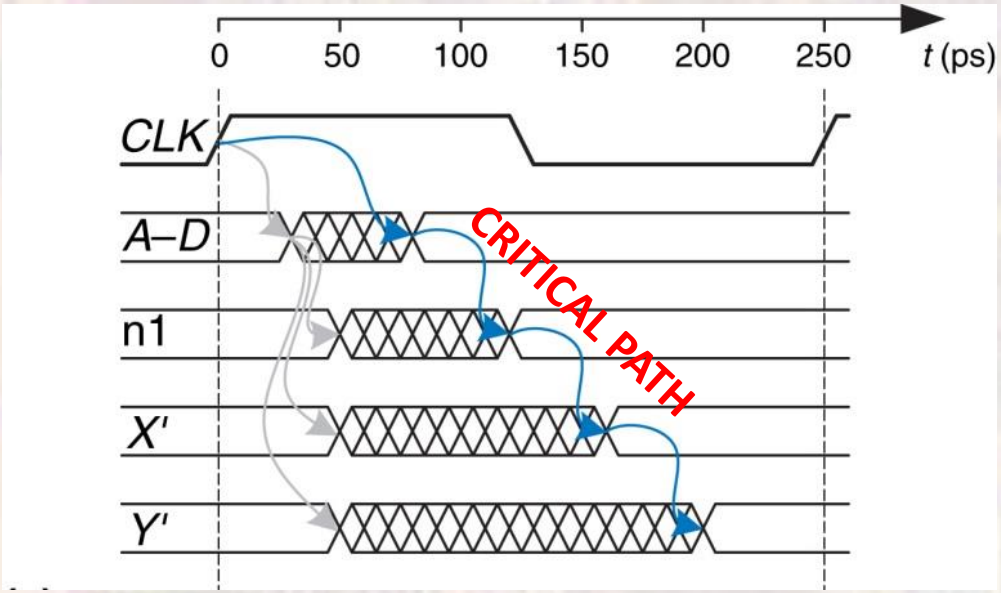
RTL Timing Analysis

- RTL Example – Critical Path

All values already account for loading



src: Harris & Harris



t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

$$t_{crit} = t_{CQ\_max} + 3*t_{pd\_max} + t_{setup}$$

$$t_{crit} = 80ps + 3*40ps + 50ps = 250ps$$

$$F_{max} = 1/250ps = 4GHz$$

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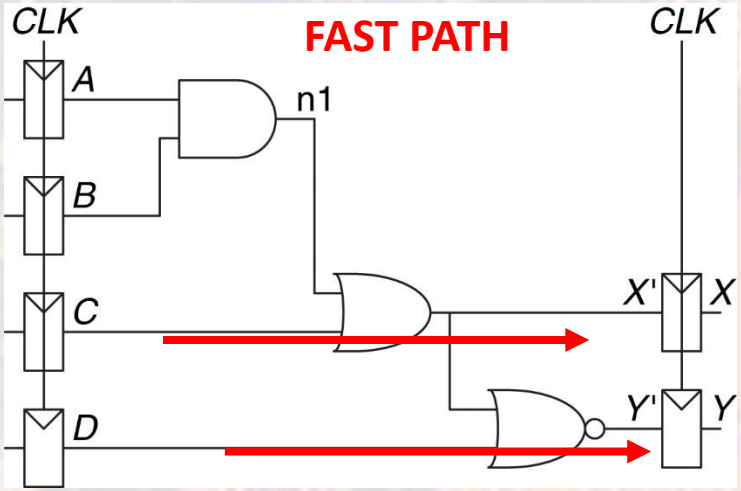
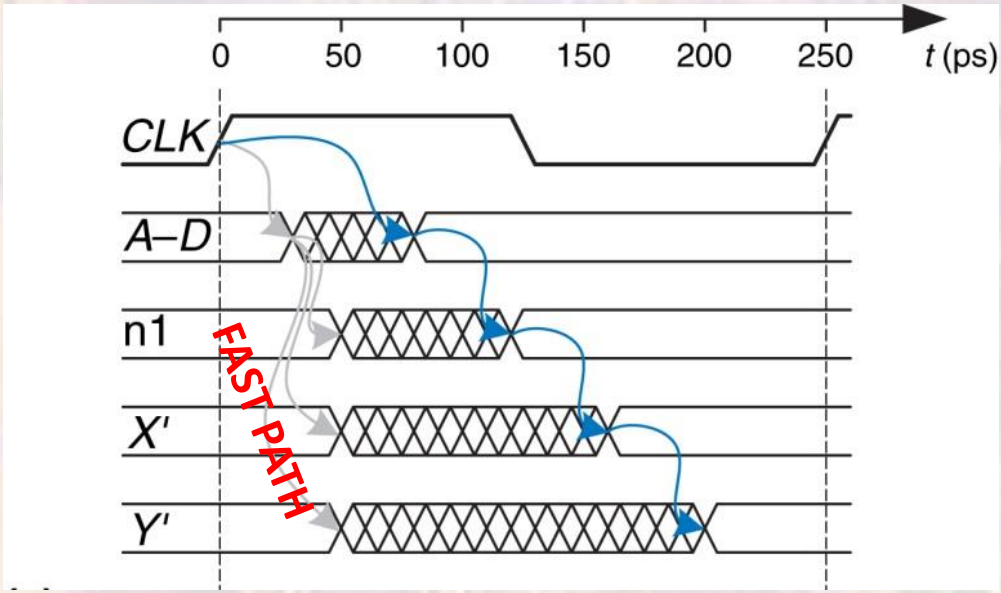
RTL Timing Analysis

- RTL Example – Fast Path

All values already account for loading



src: Harris & Harris



t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

$t'_{fast} = t_{CQ\_min} + t_{pd\_min}$

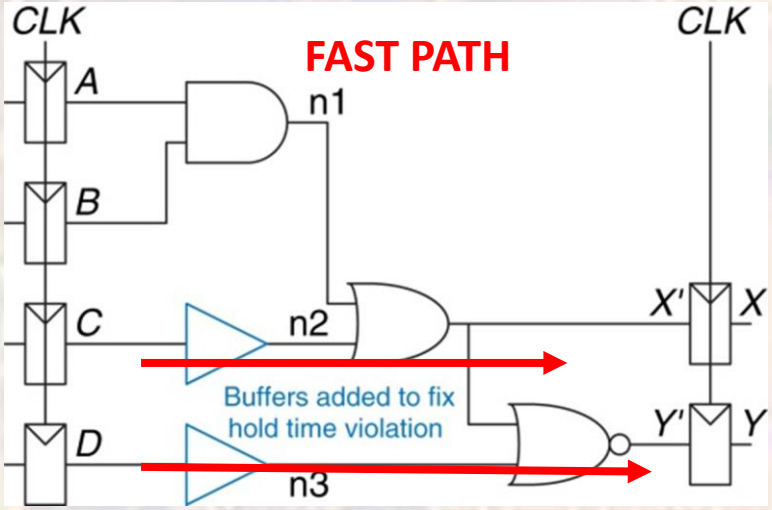
t'_{fast} = 30ps + 25ps = 55ps

t'_{fast} < hold time → unpredictable output

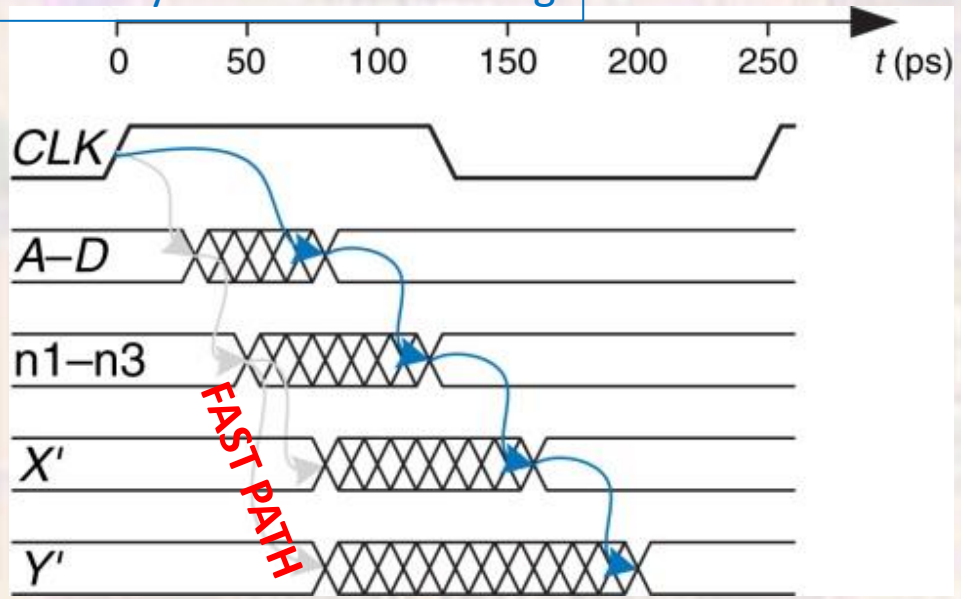
RTL Timing Analysis

- RTL Example – Fast Path - corrected

All values already account for loading



src: Harris & Harris



t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

$t'_{fast} = t_{CQ\_min} + 2*t_{pd\_min}$

t'_{fast} = 30ps + 2*25ps = 80ps

t'_{fast} > hold time → predictable output

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RTL Timing Analysis

- HOLD time reality
  - In almost all modern systems, $T_{HOLD} << T_{CQ}$ so Hold requirements rarely are a concern
  - In most integrated circuit systems, $T_{HOLD} = 0$

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RTL Timing Analysis

- Additional Timing Issues
  - Clock skew
    - Variation in clock edge arrival time
    - Due to path variations (capacitances)
    - Reduces maximum clock frequency
    - Can create hold time issues
  - Clock Gating
    - Creates clock skew

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