RTL Timing Verification

Last updated 12/12/24

RTL Timing Verification

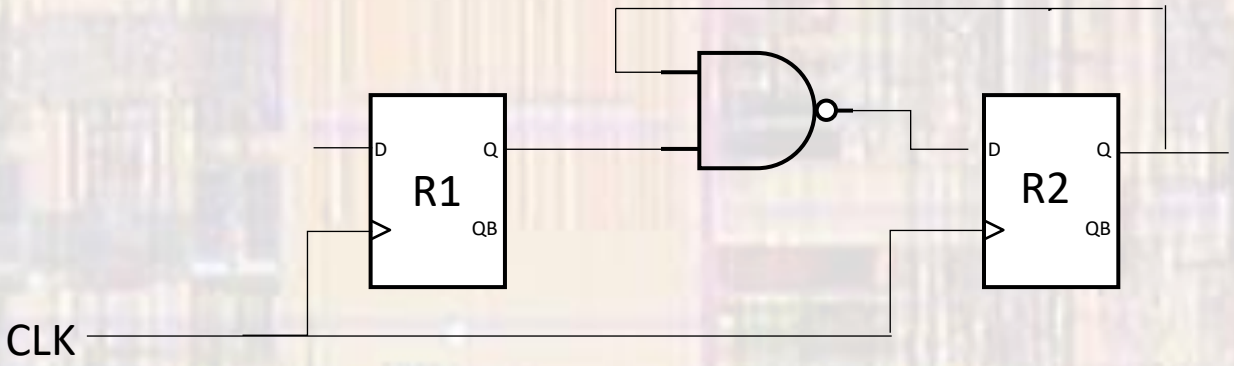
- Static Timing Analysis
  - With hundreds of inputs, millions of registers, and billions of possible states – transient timing analysis of digital circuits is practically impossible
  - Only need to determine if every register transfer can happen within a clock cycle

RTL Timing Verification

- Static Timing Analysis
  - Only need to determine if every register transfer can happen within a clock cycle
    - Check each register transfer path
    - Estimate delays based on best-case and worst-case assumptions
    - No specific input values are used
      - Logical operation IS NOT checked
    - Test for setup and hold violations
    - Create a timing analysis report

RTL Timing Verification

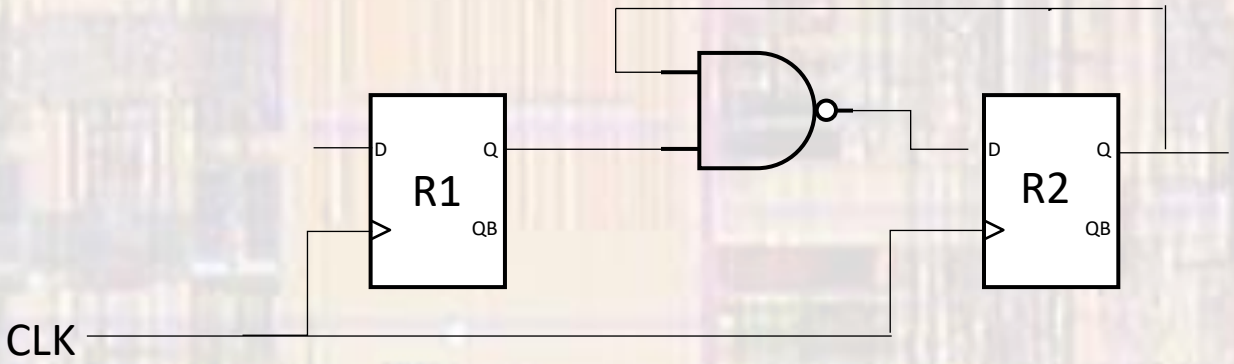
- Static Timing Analysis
  - RTL Static Timing Analysis Path
    - Input of source FlipFlop to Input of destination FlipFlop



How many static timing paths ?

RTL Timing Verification

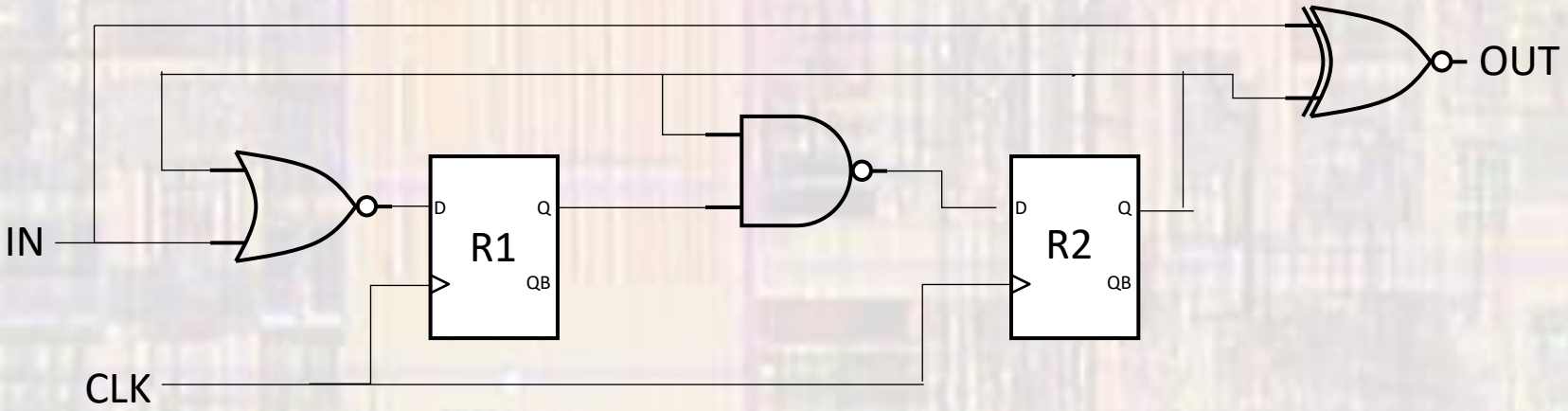
- Static Timing Analysis
  - RTL Static Timing Analysis Path
    - Input of source FlipFlop to Input of destination FlipFlop



D1 to D2
D2 to D2

RTL Timing Verification

- Static Timing Analysis
  - Complex Static Timing Analysis Path
    - Input of source FlipFlop to Input of destination FlipFlop
    - Input and Output paths



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    - Input of source FlipFlop to Input of destination FlipFlop
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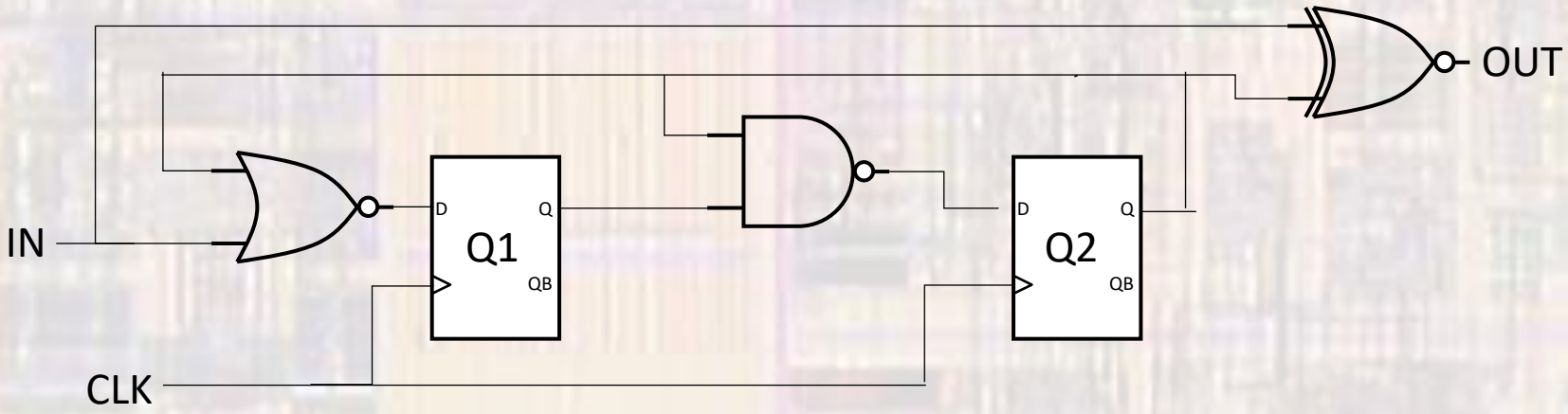

IN to D1
D1 to D2
D2 to D2
D2 to D1
D2 to OUT
IN to OUT

RTL Timing Verification

- Static Timing Analysis
  - Typical Report
    - Best-case and worst-case analysis
    - Setup time violations
    - Hold time violations

    - Reports the timing Slack
      - Slack: The gap between estimated time and time to create a violation
        - Setup Slack = Required Arrival Time (RAT) — Actual Arrival Time (AAT)
        - Hold Slack = Actual Arrival Time (AAT) — Required Arrival Time (RAT)
      - Positive Slack: The amount of time the design has to spare before failing to meet a requirement
      - Zero Slack: The design just barely meets the requirement
      - Negative Slack: The amount of time the design exceeds the requirement and fails