

Schematic Generation

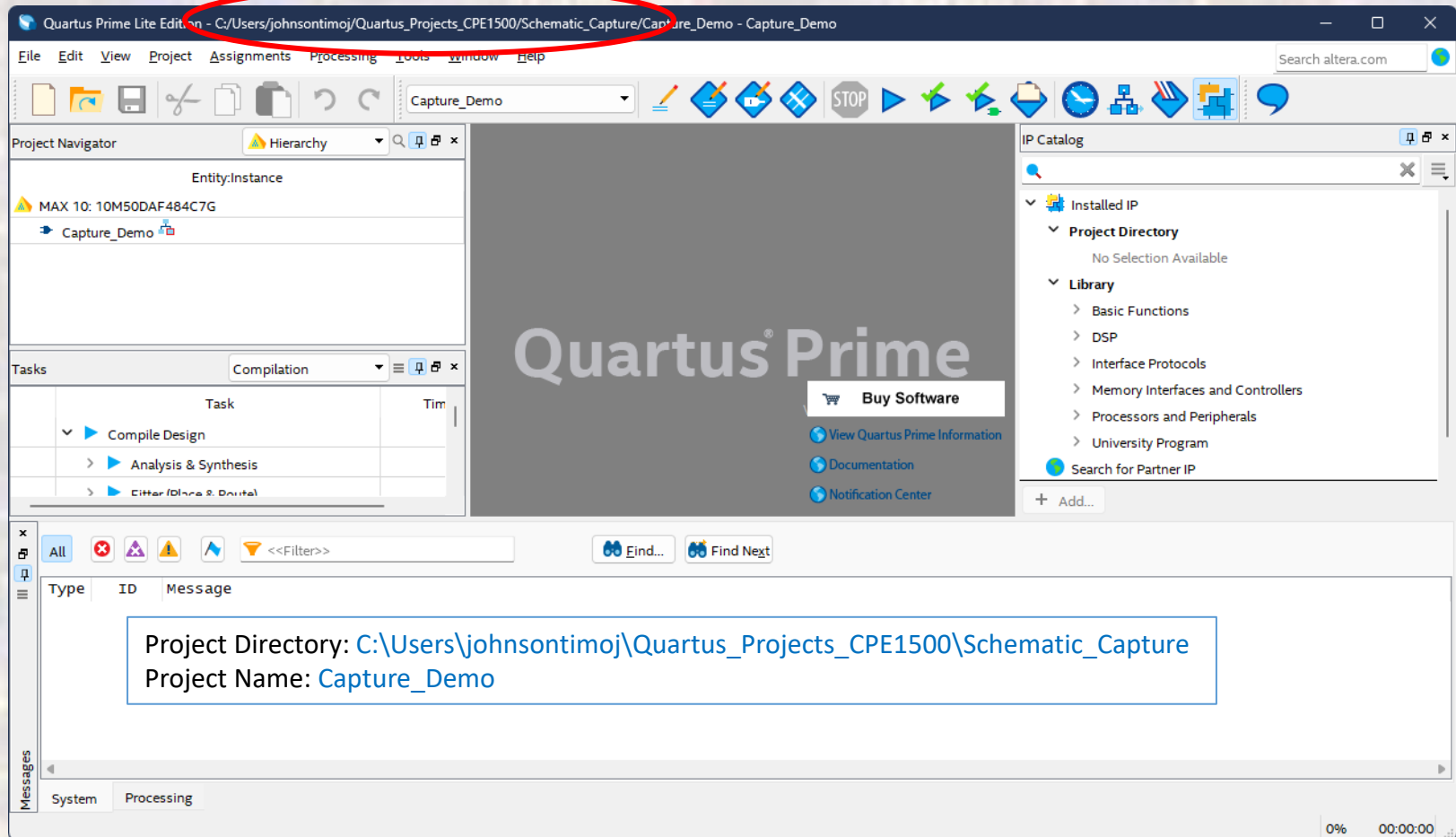
Last updated 1/13/25

Schematic Generation

- Graphical Design Capture
 - Process
 1. Create a new Quartus Project – see the [Quartus Project Setup](#) slides
 2. Open a new [Block Diagram / Schematic File](#) (BDF)
 3. Place components onto the schematic
 4. Wire the components together
 5. Add input and output pins
 6. Set [Top Level Entity](#)
 7. Run [Analysis](#) to verify connectivity

Schematic Generation

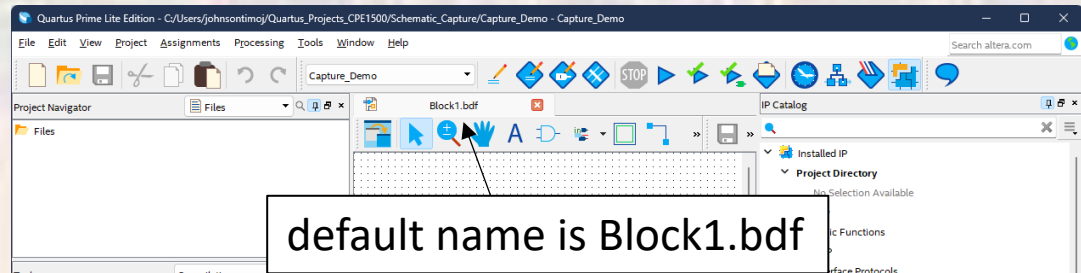
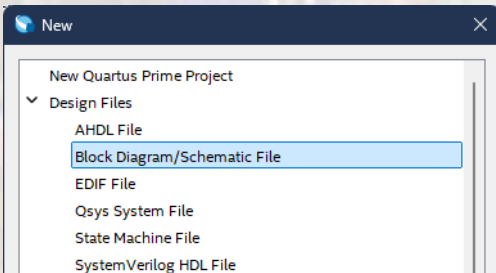
1. Create a new Quartus Project – see the [Quartus Project Setup](#) slides



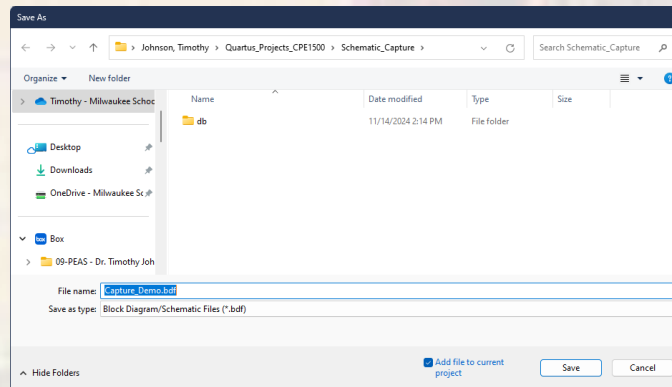
Schematic Generation

2. Open a new Block Diagram/Schematic File (BDF)

- File → New → Block Diagram/Schematic File
- OK

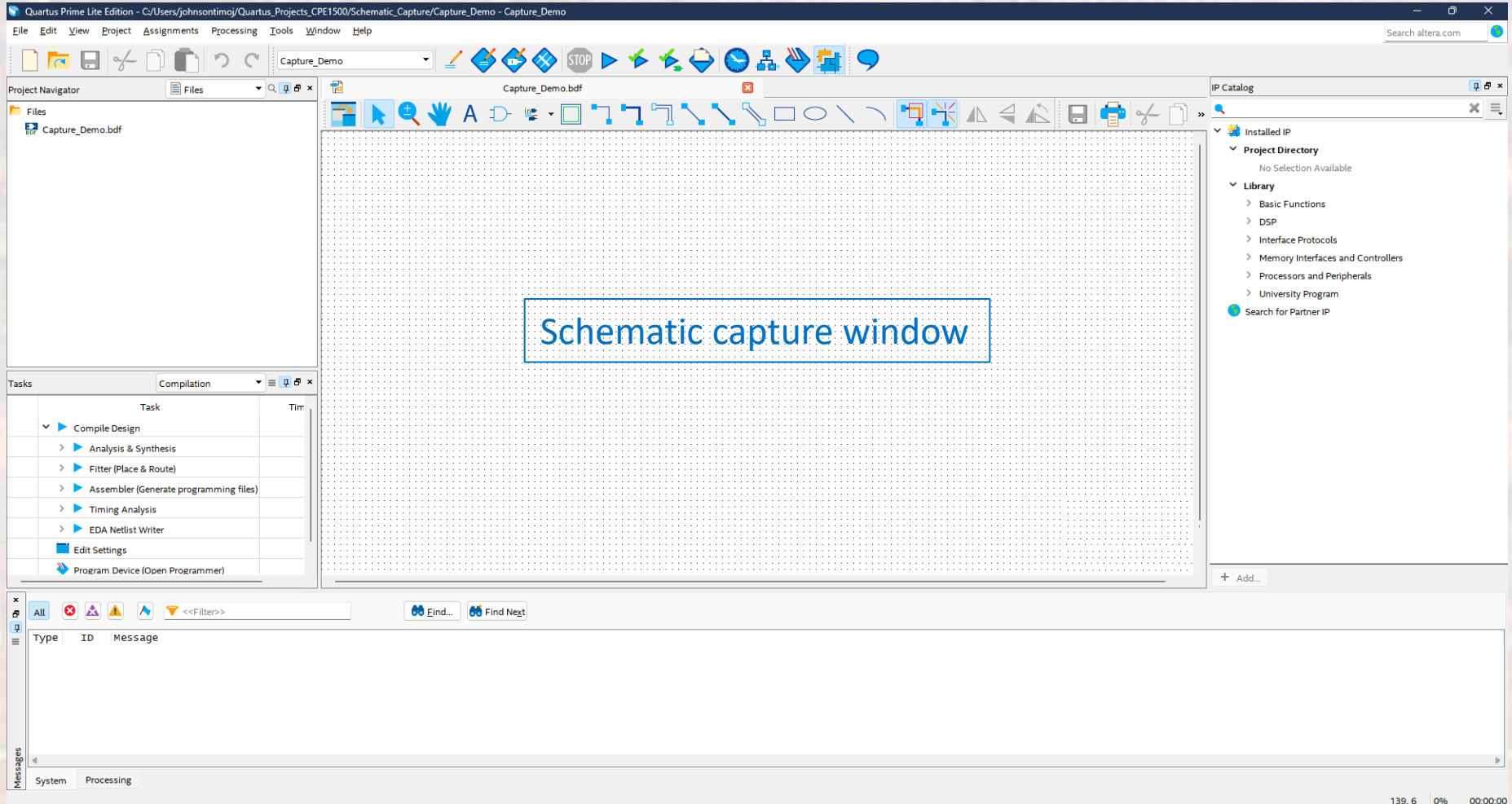


- File → Save As
 - Change the name to a descriptive name
- Save



Schematic Generation

3. Place components onto the schematic



Schematic Generation

- ## 3. Place components onto the schematic
- Select a component

The screenshot shows the Quartus Prime Lite Edition interface. The main window is a schematic capture area with a grid. A red circle highlights the 'Component' button in the top toolbar. A 'Symbol' dialog box is open, showing a tree view of libraries. The 'logic' folder is expanded, and 'and3' is selected and circled in red. The 'Name' field contains 'and3'. The 'Repeat-insert mode' checkbox is checked. The 'OK' button is circled in red. Two blue callout boxes provide instructions: 'Traverse the hierarchy to the component you want to place or Type in the name if you know it' and 'If you are placing multiple components check the box'.

Traverse the hierarchy to the component you want to place
or
Type in the name if you know it

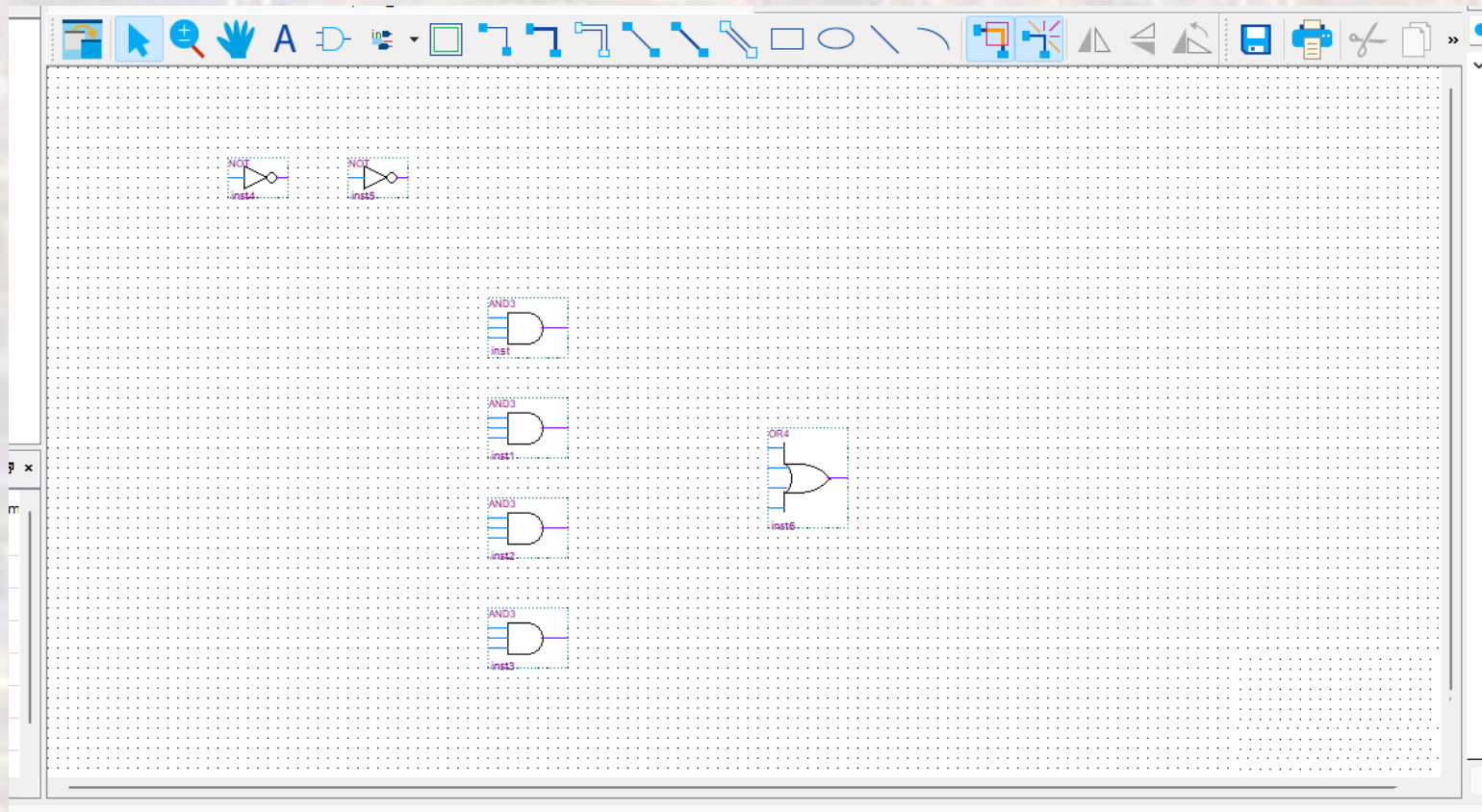
If you are placing multiple components check the box

OK Cancel

Schematic Generation

3. Place components onto the schematic

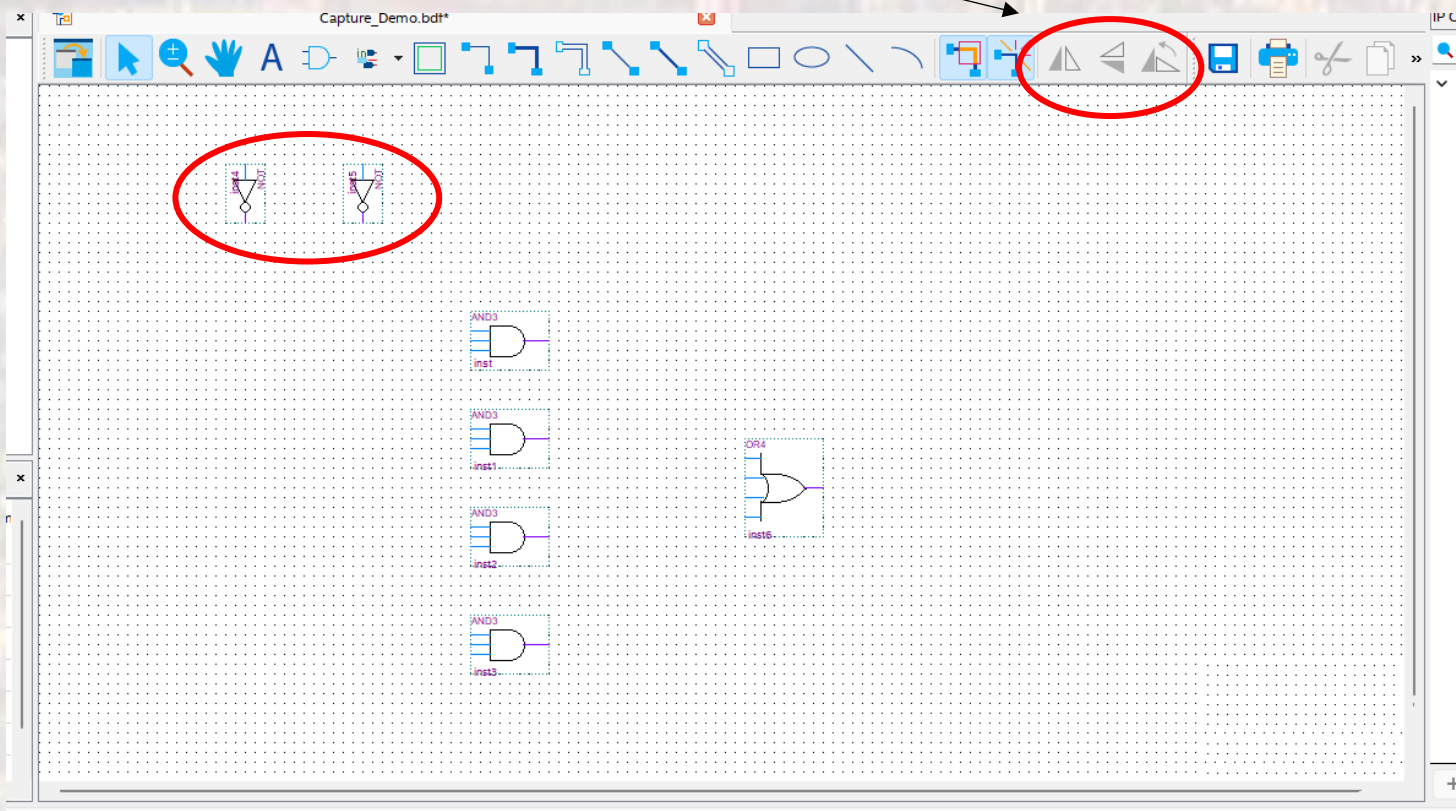
- Continue until all components are on the schematic



Schematic Generation

3. Place components onto the schematic

- You can flip / rotate components
 - Tap the component
 - Select one of these 3 options



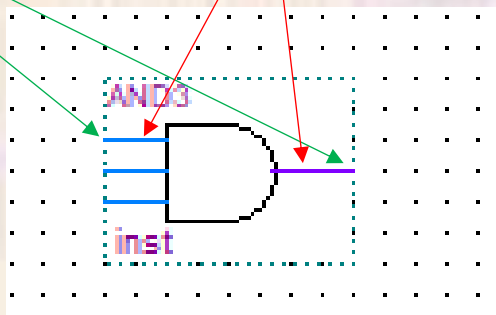
Schematic Generation

4. Wire the components together

- Component connections are ONLY at the tips of the wires on the component

connection point here

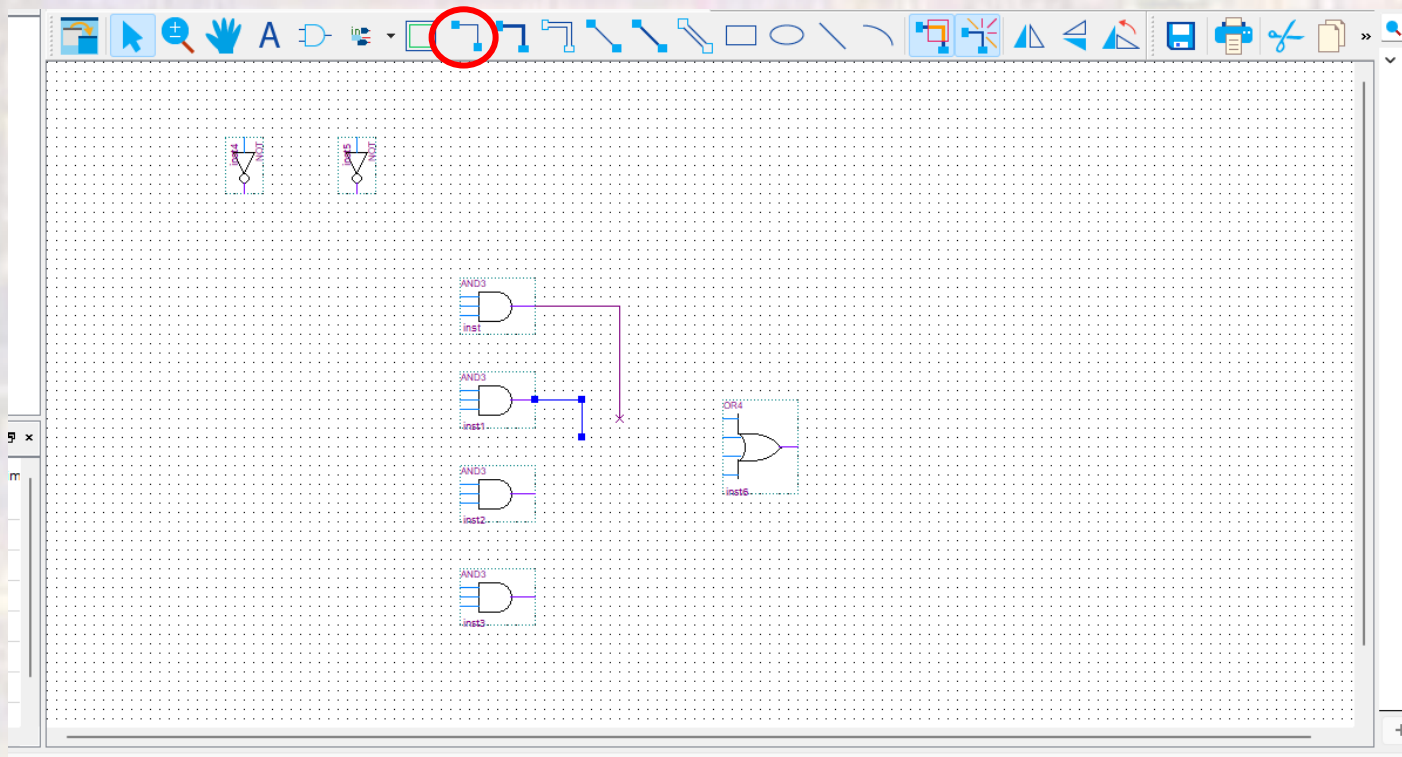
no connection point here



Schematic Generation

4. Wire the components together

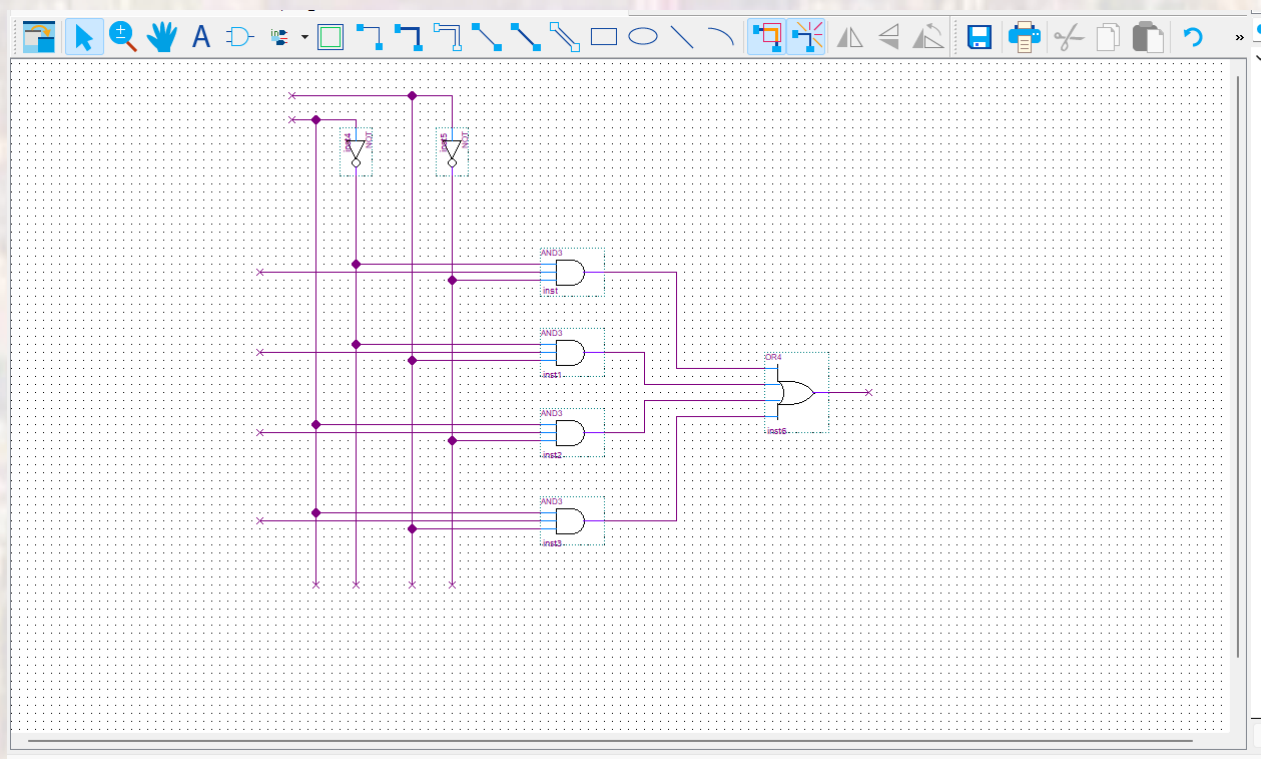
- Select the Orthogonal Wire Tool
- Click at the starting location, release at the ending location



Schematic Generation

4. Wire the components together

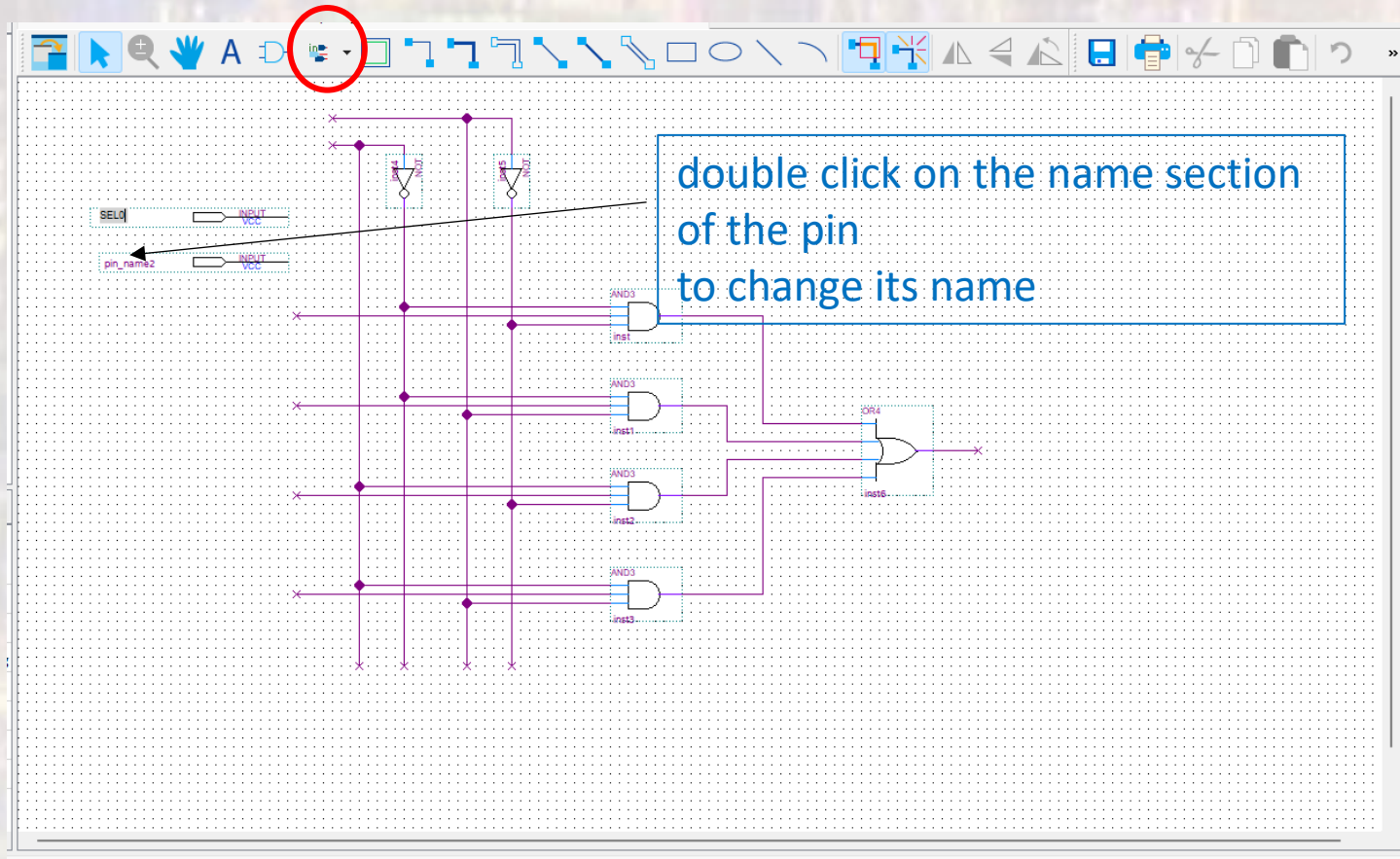
- Continue until all components are wired
- Think ahead to create a nice looking and efficient schematic



Schematic Generation

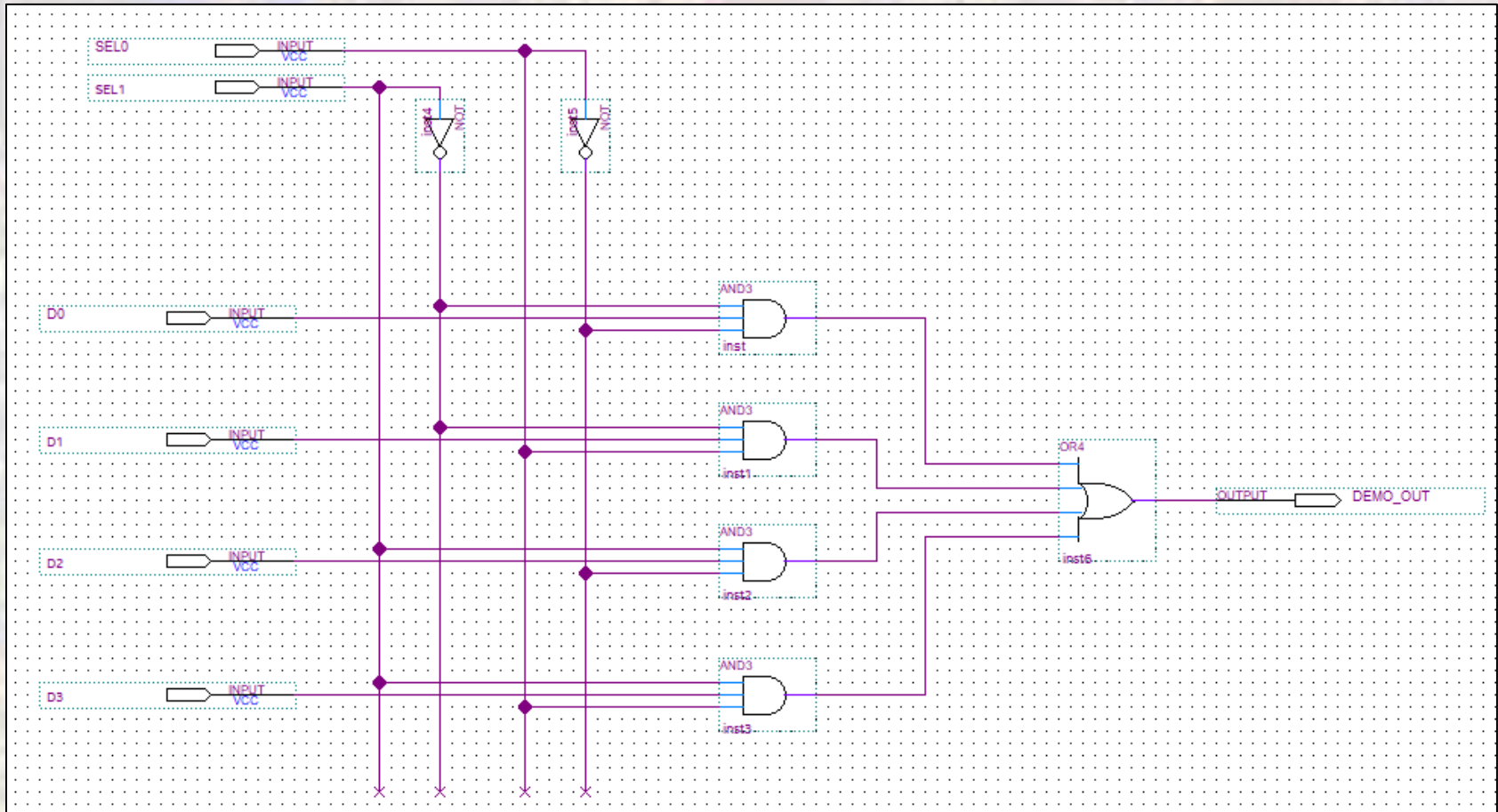
5. Add input and output pins

- Select the Pin tool and select input/output/bidir
- Change the name and wire up the pin



Schematic Generation

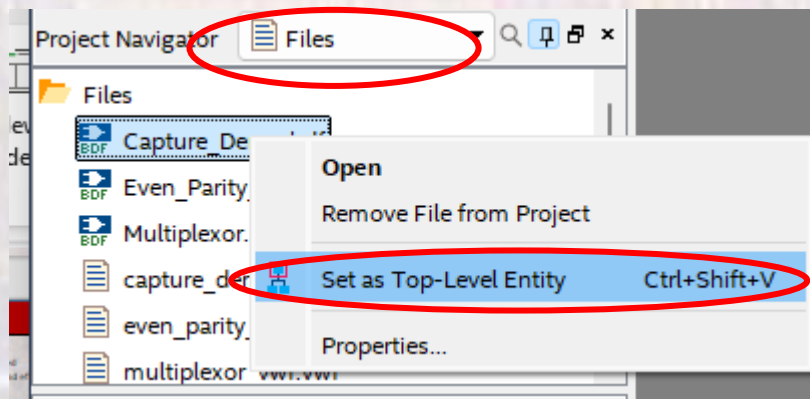
5. Add input and output pins
 - Place and wire all the pins



Schematic Generation

6. Set the Top Level Entity

- Select **Files**
- Rt-click on the design → **Set as Top Level Entity**



Schematic Generation

7. Run Analysis to verify the connections

- Processing → Analyze Current File

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows a schematic diagram of a multiplexer circuit. The circuit includes four data inputs (D0, D1, D2, D3), two select inputs (SEL0, SEL1), and a single output (OUT). Each data input is connected to a 2-to-1 multiplexer (MUX0, MUX1, MUX2, MUX3). The outputs of these MUXes are connected to a 4-to-1 multiplexer (MUX4), which produces the final output (OUT). The output is labeled as DEMO_OUT.

The Project Navigator on the left shows the project files, including Capture_Demo.bdf, Even_Parity_Generator.bdf, Multiplexor.bdf, capture_demo_vwf.vwf, even_parity_generator_vwf.vwf, and multiplexor_vwf.vwf. The Tasks window shows the compilation process, with the 'Analysis & Synthesis' task completed in 00:00:09.

The Messages window at the bottom shows the following messages:

```
Running Quartus Prime Analyze Current File
Command: quartus_map --read_settings_files=on --write_settings_files=off Capture_Demo -c Capture_Demo --analyze_file=c:/users/johnsonimj/quartus_projects_cpe1500/schematic_capture/capture_demo.bdf
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
20030 Parallel compilation is disabled and will use 20000 processors detected
Quartus Prime Analyze Current File was successful. 0 errors, 2 warnings
```

285,631 100% 00:00:10