

Schematic Simulations University Waveforms

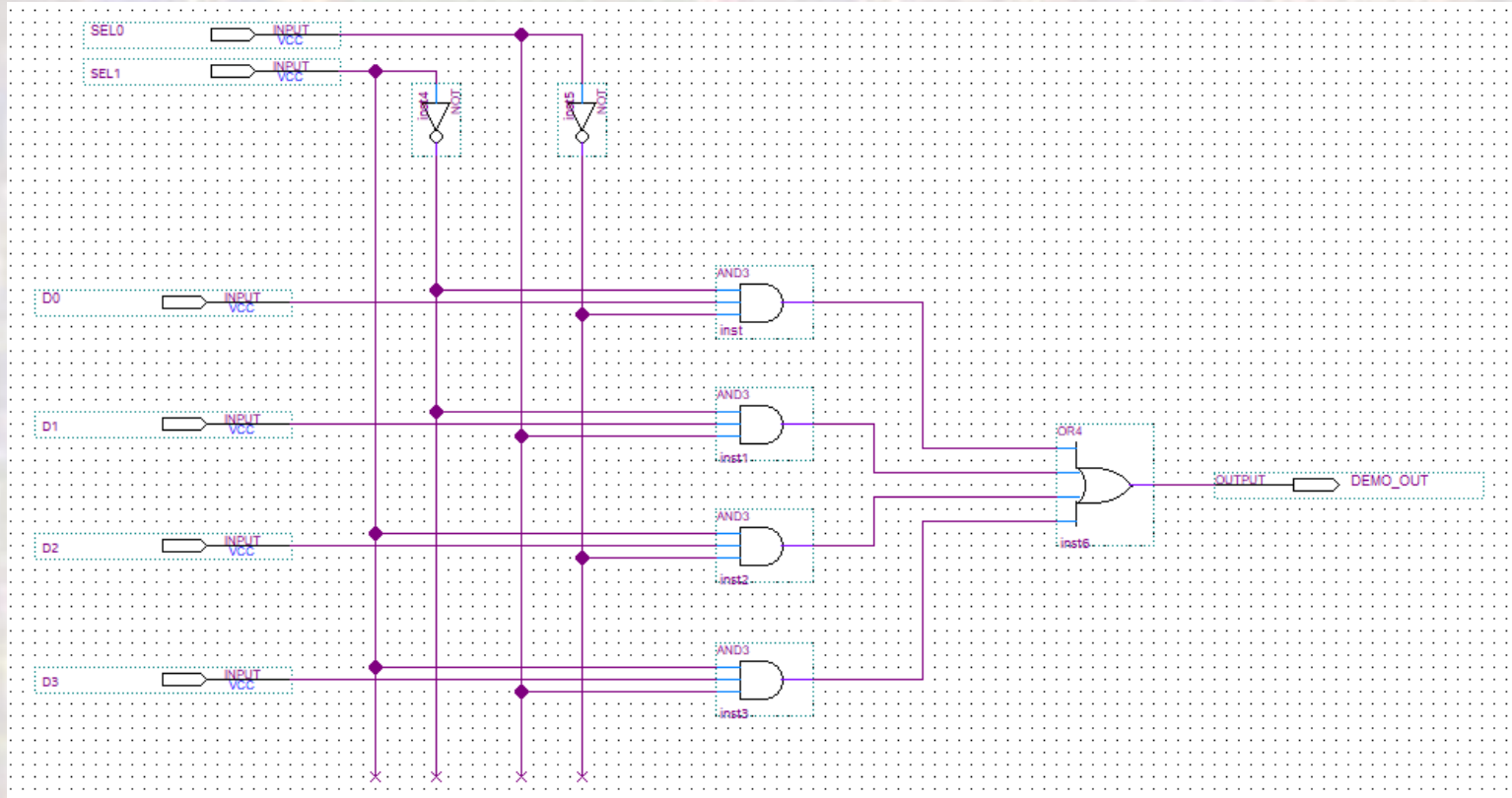
Last updated 1/29/25

Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 1. Create the schematic
 2. Run **Analysis and Synthesis** in Quartus
 3. Verify the RTL is what is expected
 4. Open a new **University Program VWF** file
 5. Select the desired signals to drive / analyze
 6. Setup the input signal waveforms
 7. Setup simulator options
 8. Run the simulation
 9. Evaluate the results

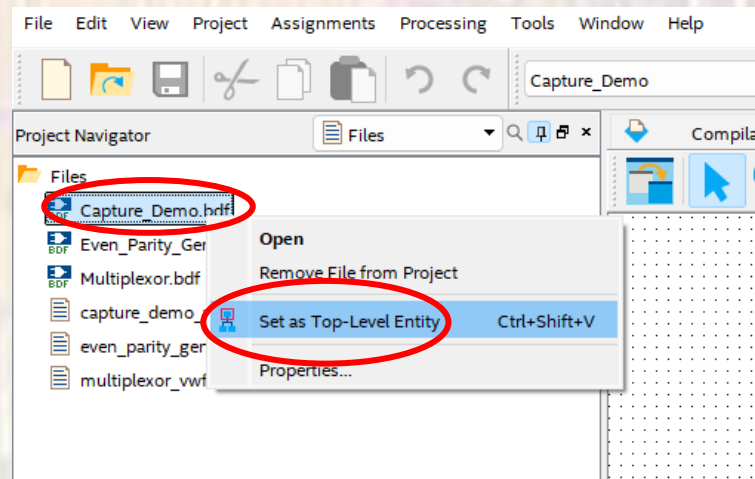
Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 1. Create the schematic
See the [Schematic Generation](#) slides



Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 2. Run **Analysis and Synthesis** in Quartus
 - Converts the schematic components to Quartus components
 - Set the top-level block
 - Rt-click on your top level block
 - Select **Set as Top-level Entity**



Schematic Simulation – University Waveforms

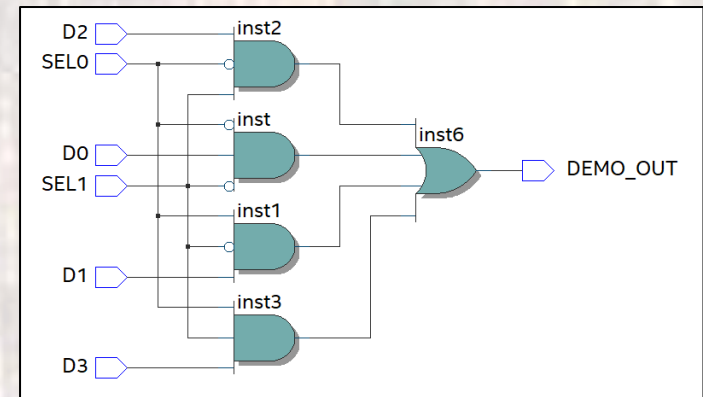
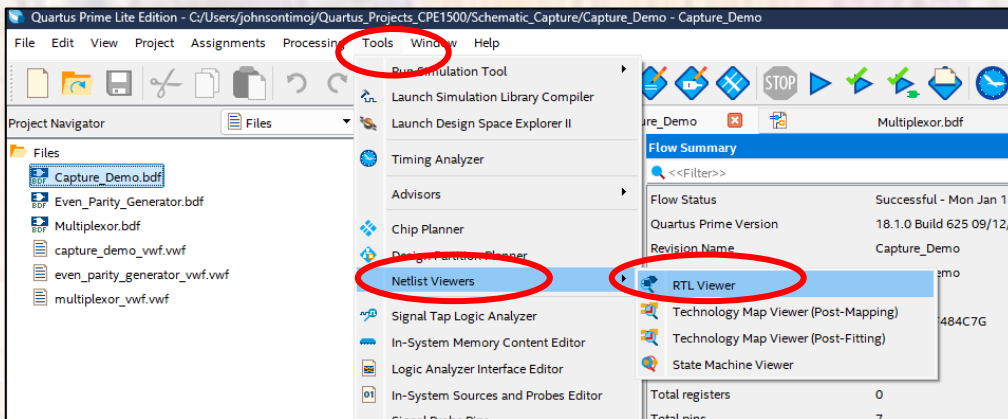
- Simulation using the University Waveform tool
 2. Run **Analysis and Synthesis** in Quartus
 - **Processing** → **Start** → **Start Analysis and Synthesis**
 - Check the **Device**
 - Check the **Top-level Entity Name**

```
286030 Timing-Driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 9 device resources after synthesis - the final resource count might be different
Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings
```

Flow Summary	
«Filter»	
Flow Status	Successful - Mon Jan 13 12:12:40 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Capture_Demo
Top-level Entity Name	Capture_Demo
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2
Total registers	0
Total pins	7
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

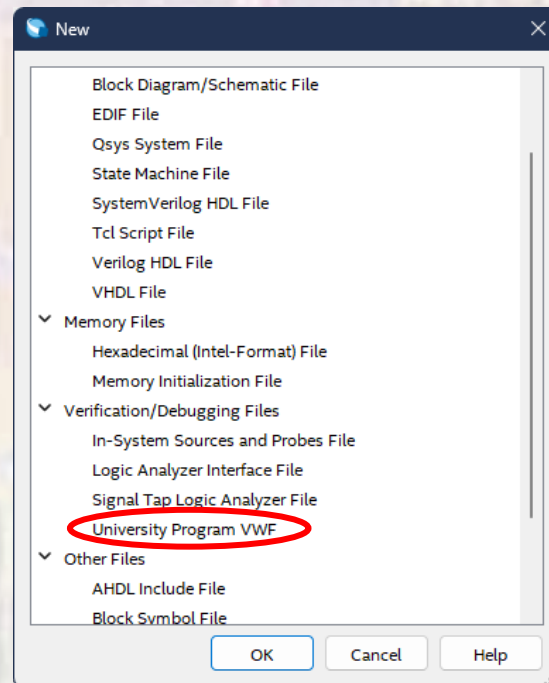
Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 3. Verify the RTL (schematic of the implementation)
 - Tools → Netlist Viewers → RTL Viewer
 - Evaluate the schematic – does it make sense?



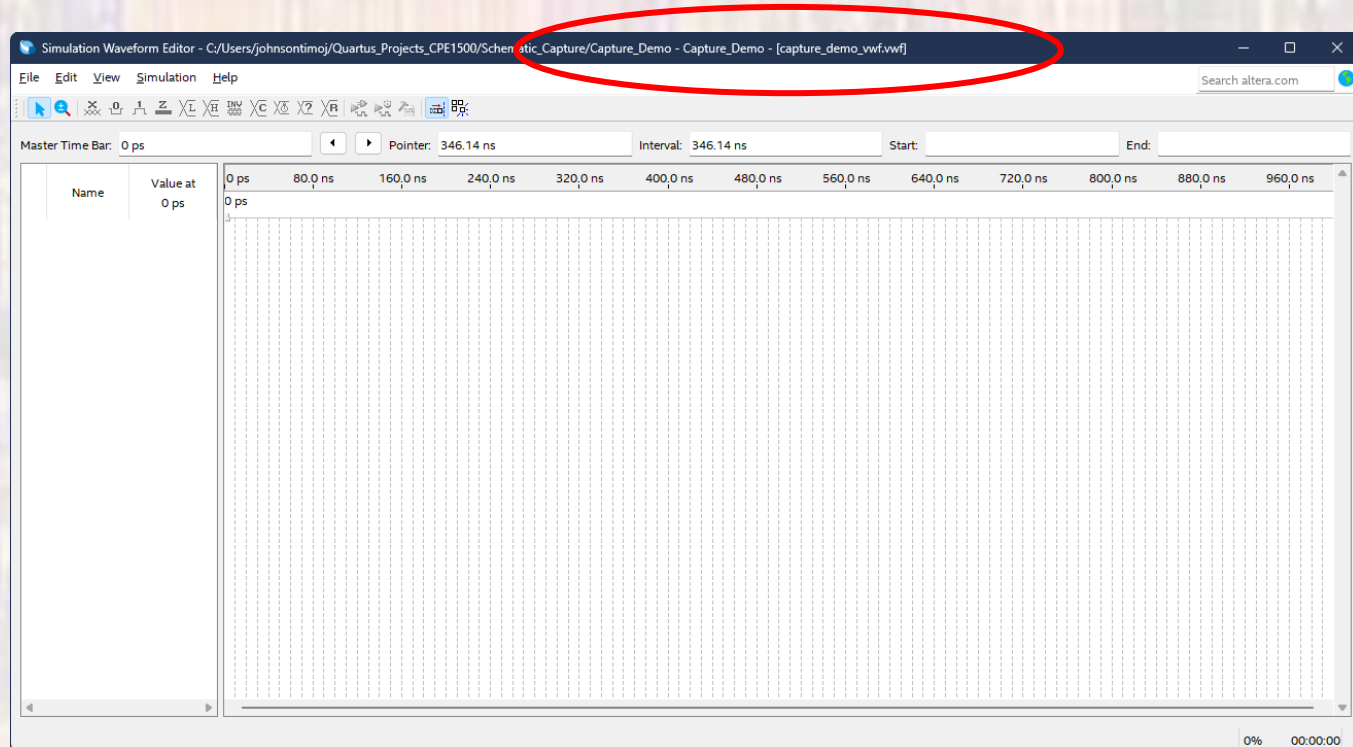
Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 4. Open a new **University Program VWF** file
 - **File** → **New** → **University Program VWF**



Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 4. Open a new **University Program VWF** file
 - File → New → University Program VWF
 - Save the file: **File** → **Save As**
 - Give is a useful file name (capture_demo_vwf.vwf)



Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 5. Select the desired signals to drive / analyze
 - Edit → Insert Node or Bus
 - Node Finder...
 - List

At this point we will only see the pins

The first screenshot shows the 'Simulation Waveform Editor' menu with 'Insert' and 'Insert Node or Bus...' circled in red. A red arrow points to the 'Insert Node or Bus' dialog box, which has 'Node Finder...' circled in red. A second red arrow points to the 'Node Finder' dialog box, where the 'List' button is circled in red. A third red arrow points to the 'Node Finder' dialog box showing a list of pins.

Node Finder (Second Screenshot):

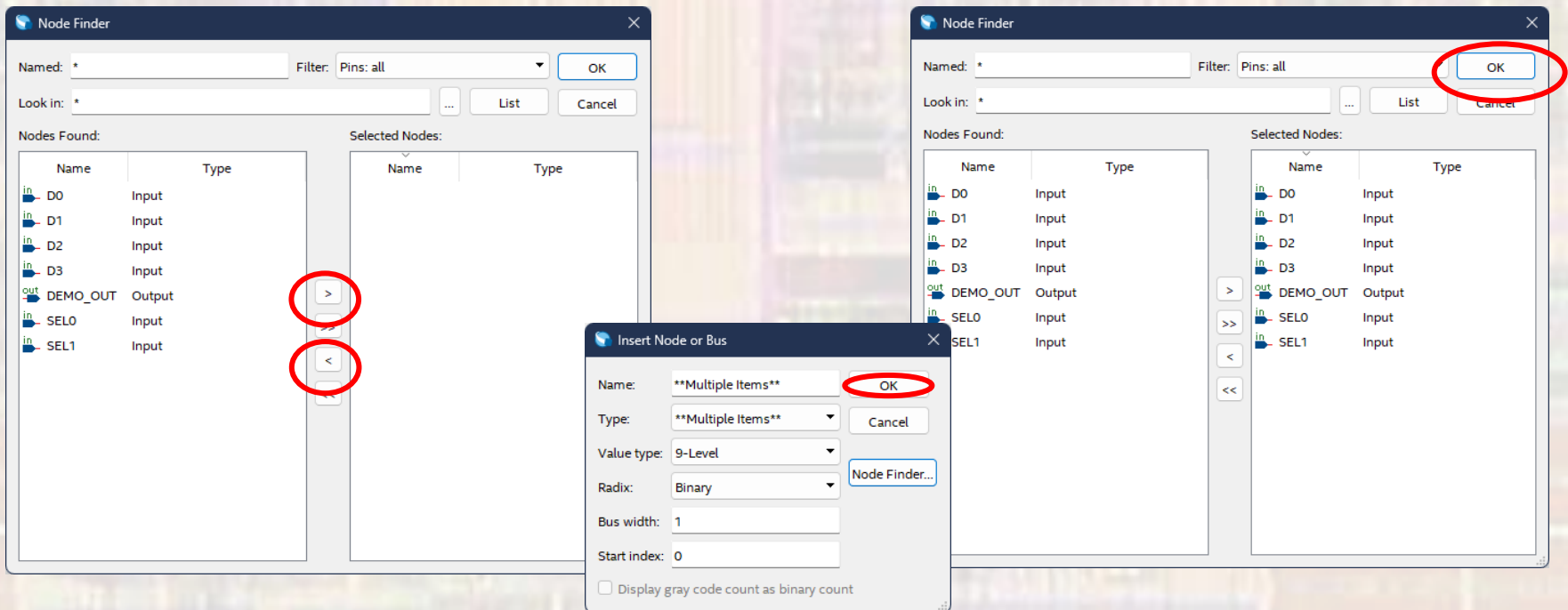
Name	Type
in_ D0	Input
in_ D1	Input
in_ D2	Input
in_ D3	Input
out_ DEMO_OUT	Output
in_ SEL0	Input
in_ SEL1	Input

Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool

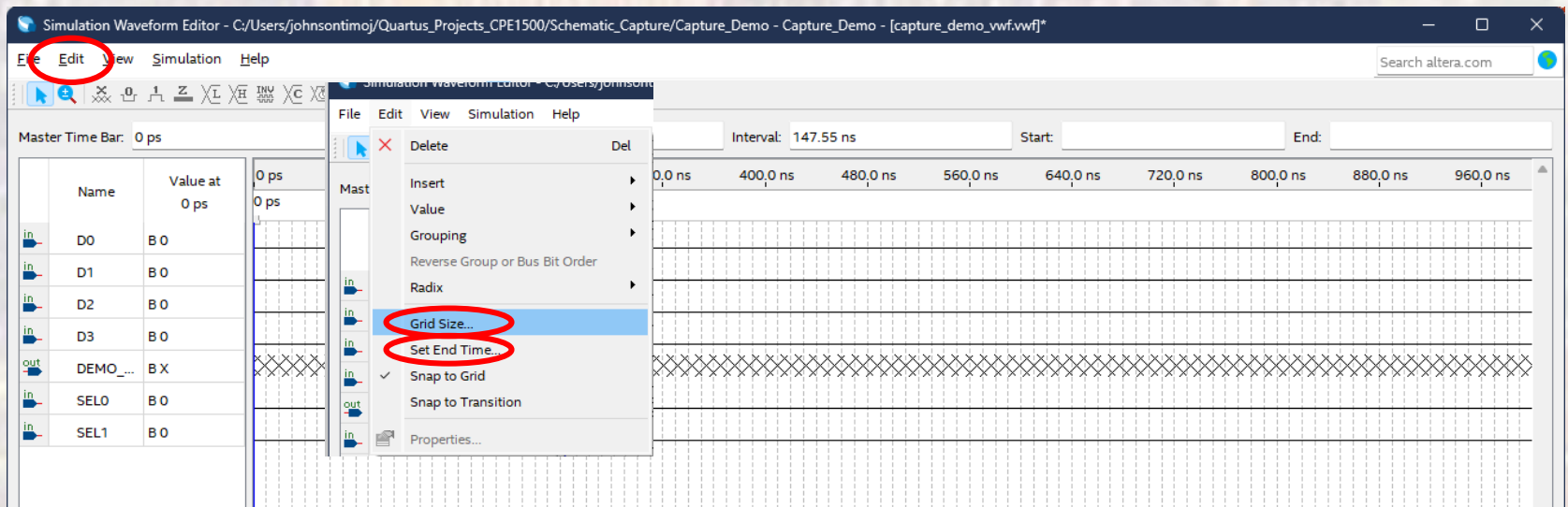
- 5. Select the desired signals to drive / analyze

- Touch a Node (Name)
- Use the arrows to move nodes from the Found list to the Selected list
- OK, OK



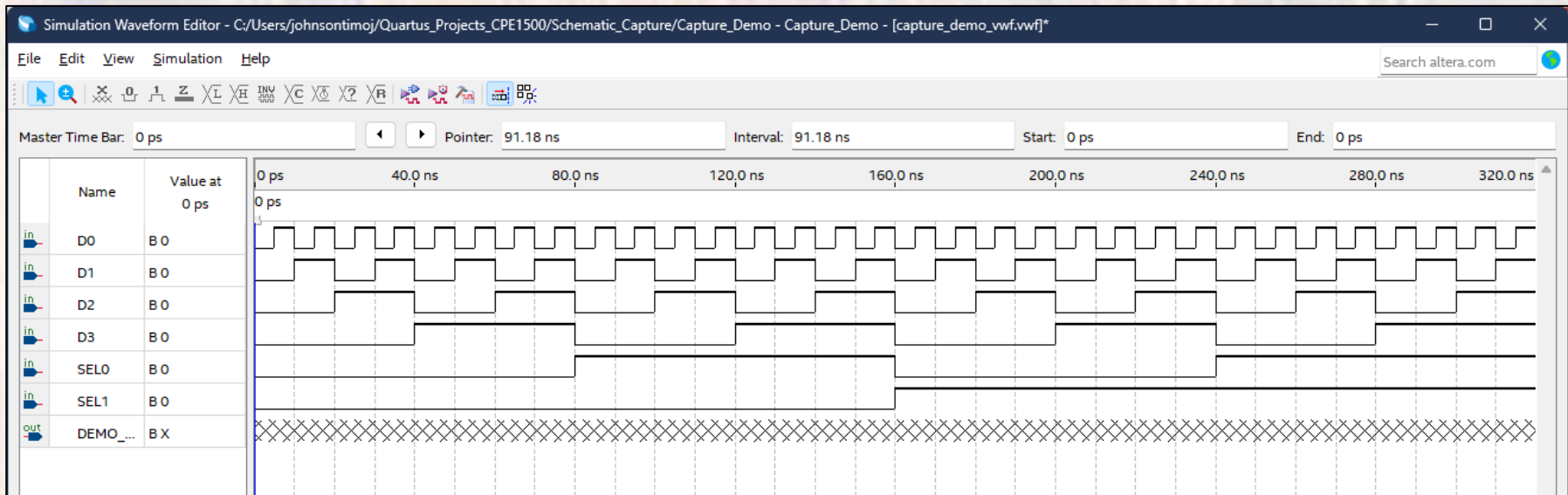
Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 6. Setup the input signal waveforms
 - You must have a plan
 - What signals to switch at what time
 - How long does the total test take
 - Edit → Set Grid Size (10 ns)
 - Edit → Set End Time (640 ns)



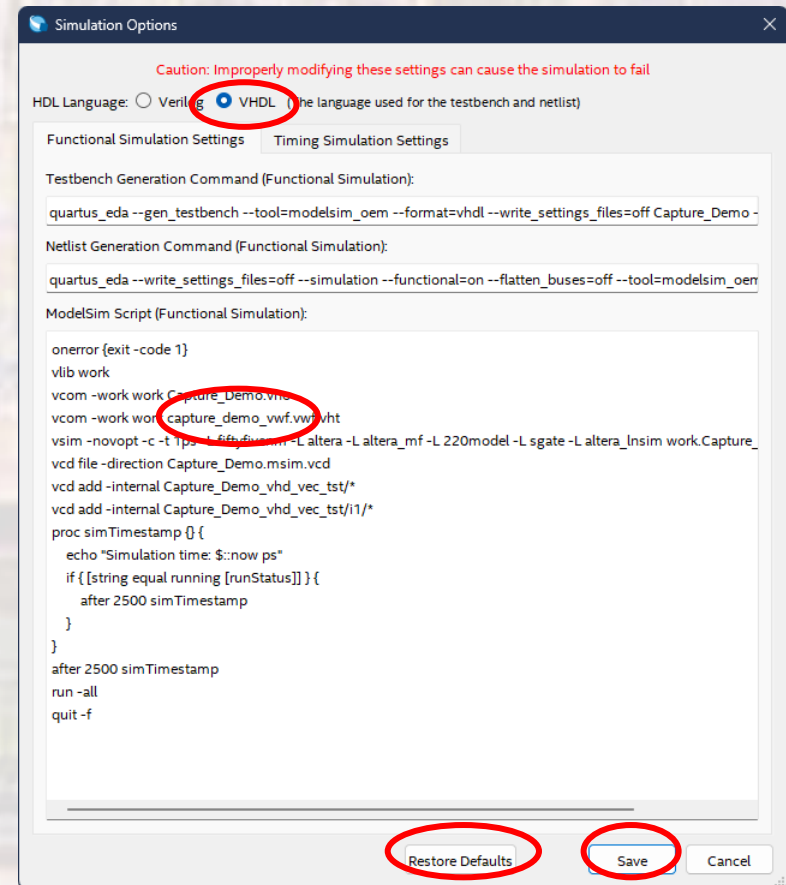
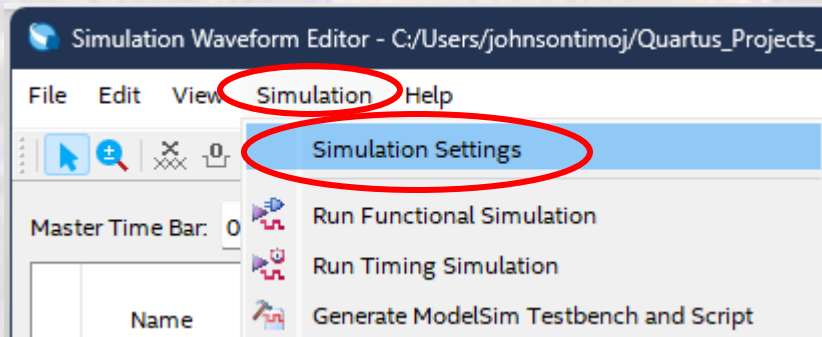
Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 5. Setup the input signal waveforms
 - See the [University Waveform Viewer – Input Setup Slides](#)
 - **File** → **Save**



Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 7. Setup the simulator options
 - Simulation → Simulation Settings
 - Select VHDL
 - Verify the vwf file name
 - If incorrect Restore Defaults
 - Save



Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 8. Run Simulation
 - Simulation → Run Functional Simulation

The screenshot shows the Quartus Simulation Waveform Editor interface. The 'Simulation' menu is open, and 'Run Functional Simulation' is highlighted. Below the menu, a 'Simulation Flow Progress' dialog box is visible, showing the progress of generating the netlist. The main window displays a simulation plot with multiple digital signals over time, ranging from 0 ns to 320.0 ns. The plot shows several signals with varying pulse widths and frequencies.

Simulation Flow Progress

```
Generating netlist...  
vector_source=C:/Users/johnsontimoi/Quartus_Projects_CPE1500/Schematic_Capture/capture_demo_vwf.vwf --  
testbench_file=C:/Users/johnsontimoi/Quartus_Projects_CPE1500/Schematic_Capture/simulation/qsim/
```

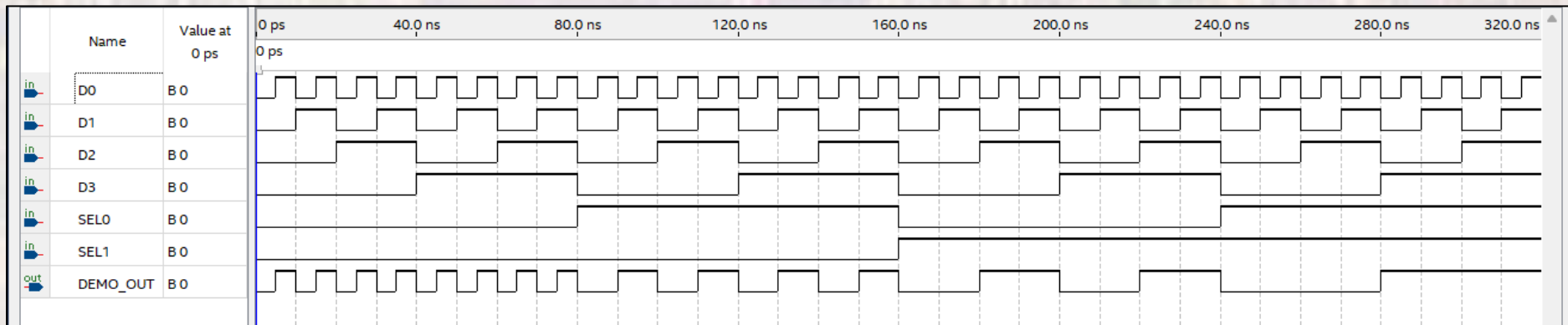
Run Log
(Will show any errors)
(Disappears if all ok)

```
**** Generating the functional simulation netlist ****  
  
quartus_eda --write_settings_files=off --simulation --functional=on --flatten_buses=off --  
tool=modelsim_oem --format=vhdl --  
output_directory="C:/Users/johnsontimoi/Quartus_Projects_CPE1500/Schematic_Capture/simulation/qsim/" Capture_Demo -c Capture_Demo
```

Simulation Plot
(not the VWF window)

Schematic Simulation – University Waveforms

- Simulation using the University Waveform tool
 9. Evaluate results
 - Compare simulation results with expected results



sel:0,0 mux: d0	sel:1,0 mux: d1	sel:1,0 mux: d2	sel:1,1 mux: d3
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ANNOTATE ANY GRAPHS TURNED IN