Last updated 1/29/25

- Simulation using the University Waveform tool
 - 1. Create the schematic
 - 2. Run Analysis and Synthesis in Quartus
 - 3. Verify the RTL is what is expected
 - 4. Open a new University Program VWF file
 - 5. Select the desired signals to drive / analyze
 - 6. Setup the input signal waveforms
 - 7. Setup simulator options
 - 8. Run the simulation
 - 9. Evaluate the results

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- Simulation using the University Waveform tool
 - 1. Create the schematic

See the Schematic Generation slides



- Simulation using the University Waveform tool
 - 2. Run Analysis and Synthesis in Quartus

Converts the schematic components to Quartus components

- Set the top-level block
 - Rt-click on your top level block
 - Select Set as Top-level Entity



- Simulation using the University Waveform tool
 - 2. Run Analysis and Synthesis in Quartus
 - Processing → Start → Start Analysis and Synthesis
 - Check the Device
 - Check the Top-level Entity Name

286030 Timing-Driven Synthesis is running
 16010 Generating hard_block partition "hard_block:auto_generated_inst"
 21057 Implemented 9 device resources after synthesis - the final resource count might be different
 Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings

	Flow Summary	
	< <filter>></filter>	
	Flow Status	Successful - Mon Jan 13 12:12:40 2025
1	Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
	Revision Name	Capture Demo
	Top-level Entity Name	Capture_Demo
	Family	MAX 10
	Device	10M50DAF484C7G
	Timing Models	Final
	Total logic elements	2
	Total registers	0
	Total pins	7
	Total virtual pins	0
	Total memory bits	0
	Embedded Multiplier 9-bit elements	0
	Total PLLs	0
	UFM blocks	0
	ADC blocks	0

- Simulation using the University Waveform tool
 - 3. Verify the RTL (schematic of the implementation)
 - Tools → Netlist Viewers → RTL Viewer
 - Evaluate the schematic does it make sense?





- Simulation using the University Waveform tool
 - 4. Open a new University Program VWF file
 - File → New → University Program VWF



- Simulation using the University Waveform tool
 - 4. Open a new University Program VWF file
 - File → New → University Program VWF
 - Save the file: File → Save As
 - Give is a useful file name (capture_demo_vwf.vwf)

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- Simulation using the University Waveform tool
 - 5. Select the desired signals to drive / analyze
 - Edit \rightarrow Insert Node or Bus
 - Node Finder...

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At this point we will only see the pins

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ix: Binary						
width: 1						
t index: 0 Display gray code count as binary count						
)		9				

- Simulation using the University Waveform tool
 - 5. Select the desired signals to drive / analyze
 - Touch a Node (Name)
 - Use the arrows to move nodes form the Found list to the Selected list
 - OK, OK

		^	Those Finder		
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Look in: *	L	ist Cancel	Look in: *		List Carro
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- Simulation using the University Waveform tool
 - 6. Setup the input signal waveforms
 - You must have a plan
 - What signals to switch at what time
 - How long does the total test take
 - Edit → Set Grid Size (10 ns)
 - Edit → Set End Time (640 ns)

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- Simulation using the University Waveform tool
 - 5. Setup the input signal waveforms
 - See the University Waveform Viewer Input Setup Slides
 - File \rightarrow Save

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- Simulation using the University Waveform tool
 - 7. Setup the simulator options
 - Simulation → Simulation Settings
 - Select VHDL
 - Verify the vwf file name
 - If incorrect Restore Defaults
 - Save



Simulation Options Caution: Improperly modifying these settings can cause the simulation to fail DL Language: O Veril (O VHDL) he language used for the testbench and netlist)
Caution: Improperly modifying these settings can cause the simulation to fail DL Language: O Veril g • VHDL the language used for the testbench and netlist)
DL Language: 🔿 Veril g 💿 VHDL ()he language used for the testbench and netlist)
Functional Simulation Settings Timing Simulation Settings
Testbench Generation Command (Functional Simulation):
quartus_edagen_testbenchtool=modelsim_oemformat=vhdlwrite_settings_files=off Capture_Demo -
Netlist Generation Command (Functional Simulation):
quartus_edawrite_settings_files=offsimulationfunctional=onflatten_buses=offtool=modelsim_oen
ModelSim Script (Functional Simulation):
<pre>onerror {exit - code 1} vlib work vcom -work work Capture_Demo.vne vcom -work work capture_demo_vwf.ww/vht vsim -novopt -c +t 1ps - <u>66p_0ur_m</u> +t altera - L altera_mf -L 220model -L sgate -L altera_Insim work.Capture_ vcd file -direction Capture_Demo_vhd_vec_tst/* vcd add -internal Capture_Demo_vhd_vec_tst/* vcd add -internal Capture_Demo_vhd_vec_tst/i1/* proc sim Timestamp {{ echo *Simulation time: \$::now ps* if {[string equal running [runStatus]]}{ after 2500 sim Timestamp } } after 2500 sim Timestamp run -all quit -f</pre>

Restore Default

Save

Cancel

- Simulation using the University Waveform tool
 - 8. Run Simulation
 - Simulation → Run Functional Simulation

Simulation Waveform Editor - C:/Users/jo	ohnsontimoj/Quartus_Projects_C					
File Edit View simulation Help						
Simulation Setting	gs					
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Name Run Timing Simul	m Testbench and Script	5 X2 X8 📌 🤁 📾 🎼				Search altera.com
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<pre>**** Generating the functional simulation netlist **** quartus_edawrite_settings_files=offsimulationfunction tool=modelsim_oemformat=vhdl output_directory="C;/Users/johnsontimoj/Quartus_Projects_ /qsim/" Capture_Demo -c Capture_Demo</pre>	nal=onflatten_buses=off .CPE1500/Schematic_Capture/simula	tion		Simula (not the V	tion Plot WF window)	

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- Simulation using the University Waveform tool
 - 9. Evaluate results
 - Compare simulation results with expected results



ANNOTATE ANY GRAPHS TURNED IN