

# Schematic to DE10

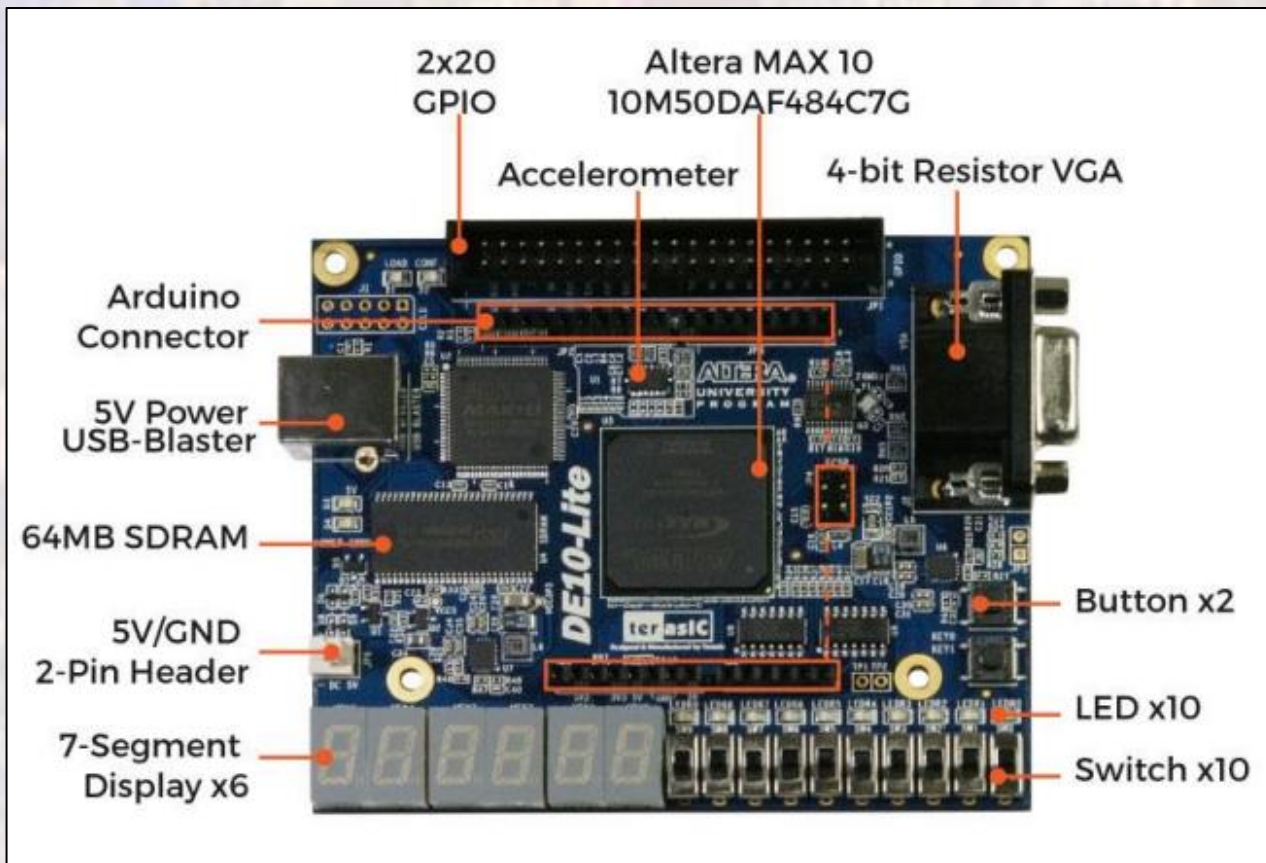
Last updated 1/29/25

# Schematic to DE10

- Verification via Hardware (DE10)
  1. Create the schematic
    - see [Quartus Schematic Generation](#) slides
  2. Verify the design via simulation
    - see the [Schematic Simulation University Waveforms](#) slides
  3. Plan the DE10 locations for each pin on the schematic
  4. Map the schematic pins to DE10 inputs and outputs
  5. Compile the design
  6. Download the design to the DE10
  7. Verify the design

# Schematic to DE10

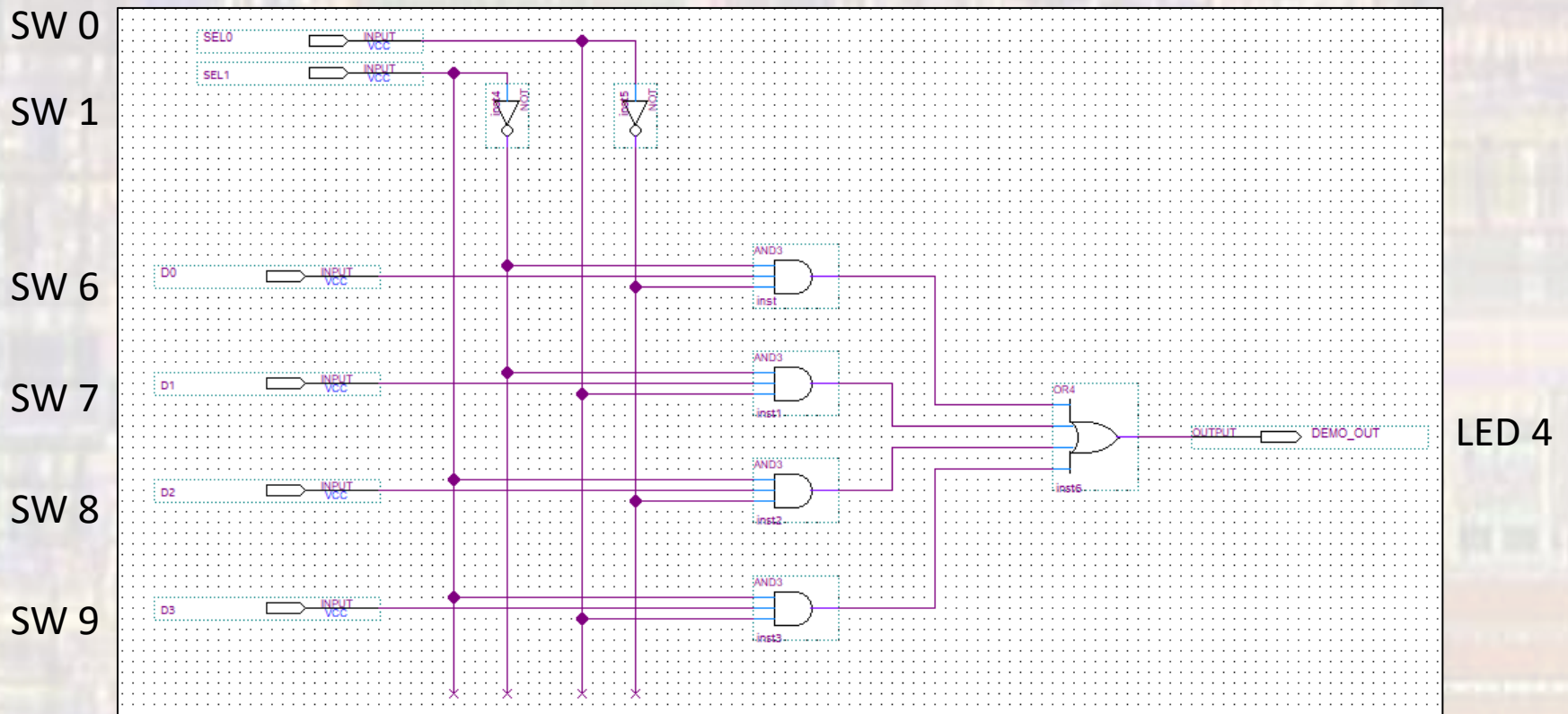
3) Plan the DE10 locations for each pin on the schematic



9 SW and LED 0

# Schematic to DE10

3) Plan the DE10 locations for each pin on the schematic



# Schematic to DE10

## 4) Map the schematic pins to DE10 inputs and outputs

sel0  
sel1  
  
d0  
d1  
d2  
d3

**Table 3-4 Pin Assignment of Slide Switches**

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTTL

demo\_out

**Table 3-5 Pin Assignment of LEDs**

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTTL

# Schematic to DE10

4) Map the schematic pins to DE10 inputs and outputs

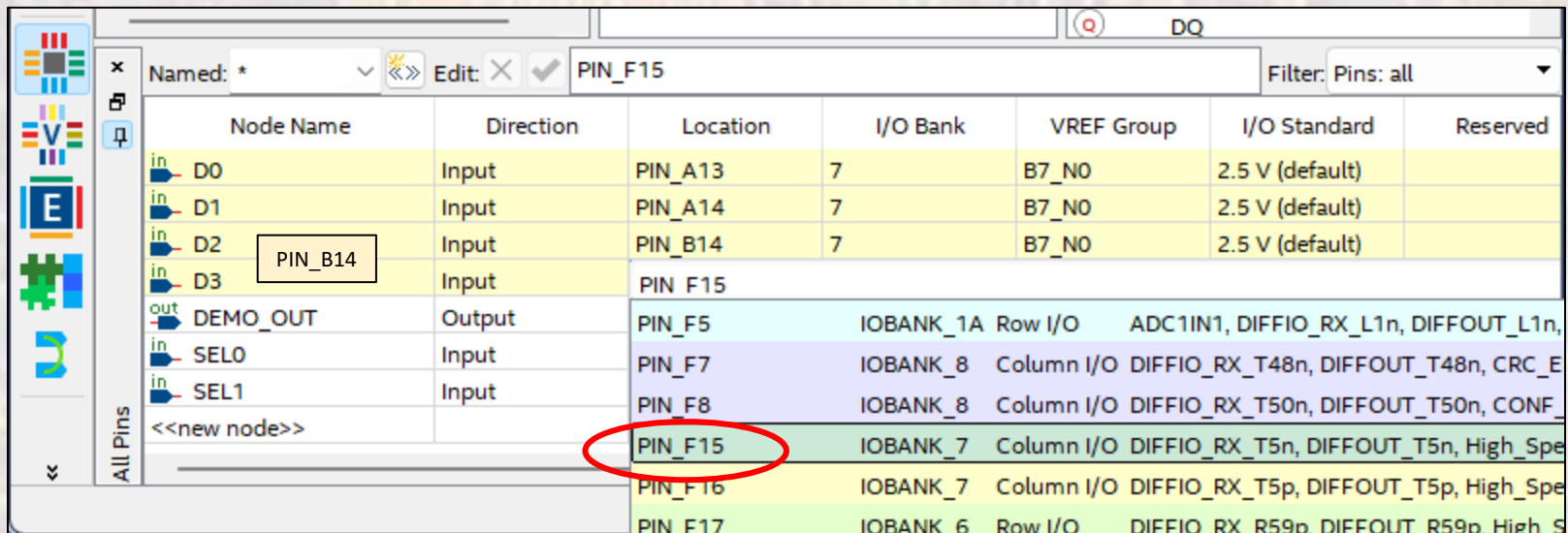
- Assignments → Pin Planner

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
in D0	Input				2.5 V (default)	Reserved
in D1	Input				2.5 V (default)	
in D2	Input				2.5 V (default)	
in D3	Input				2.5 V (default)	
out DEMO_OUT	Output				2.5 V (default)	
in SEL0	Input				2.5 V (default)	
in SEL1	Input				2.5 V (default)	
<<new node>>						

# Schematic to DE10

## 4) Map the schematic pins to DE10 inputs and outputs

- Double click on the location column for a pin
- Select the expand arrow
- Scroll until the desired pin is found and select it
- Close the Pin Planner when finished



The screenshot shows the Pin Planner interface with a table of nodes and their connections. The table has the following columns: Node Name, Direction, Location, I/O Bank, VREF Group, I/O Standard, and Reserved. The 'PIN\_F15' row is circled in red.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
in D0	Input	PIN_A13	7	B7_NO	2.5 V (default)	
in D1	Input	PIN_A14	7	B7_NO	2.5 V (default)	
in D2	Input	PIN_B14	7	B7_NO	2.5 V (default)	
in D3	Input	PIN F15				
out DEMO_OUT	Output	PIN_F5	IOBANK_1A	Row I/O	ADC1IN1, DIFFIO_RX_L1n, DIFFOUT_L1n,	
in SEL0	Input	PIN_F7	IOBANK_8	Column I/O	DIFFIO_RX_T48n, DIFFOUT_T48n, CRC_E	
in SEL1	Input	PIN_F8	IOBANK_8	Column I/O	DIFFIO_RX_T50n, DIFFOUT_T50n, CONF_	
<<new node>>		PIN_F15	IOBANK_7	Column I/O	DIFFIO_RX_T5n, DIFFOUT_T5n, High_Spe	
		PIN_F16	IOBANK_7	Column I/O	DIFFIO_RX_T5p, DIFFOUT_T5p, High_Spe	
		PIN_F17	IOBANK_6	Row I/O	DIFFIO_RX_R59p, DIFFOUT_R59p, High_S	

# Schematic to DE10

## 5) Compile the design

- Save
- Right click on the design and select Set as Top-Level Entity
- Processing → Start Compilation
- Verify success

Flow Summary	
Filter <<Filter>>	
Flow Status	Successful - Mon Jan 13 12:49:49 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Capture_Demo
Top-level Entity Name	Capture_Demo
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Pin
Total logic elements	3 / 49,760 (< 1 %)
Total registers	0
Total pins	7 / 360 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

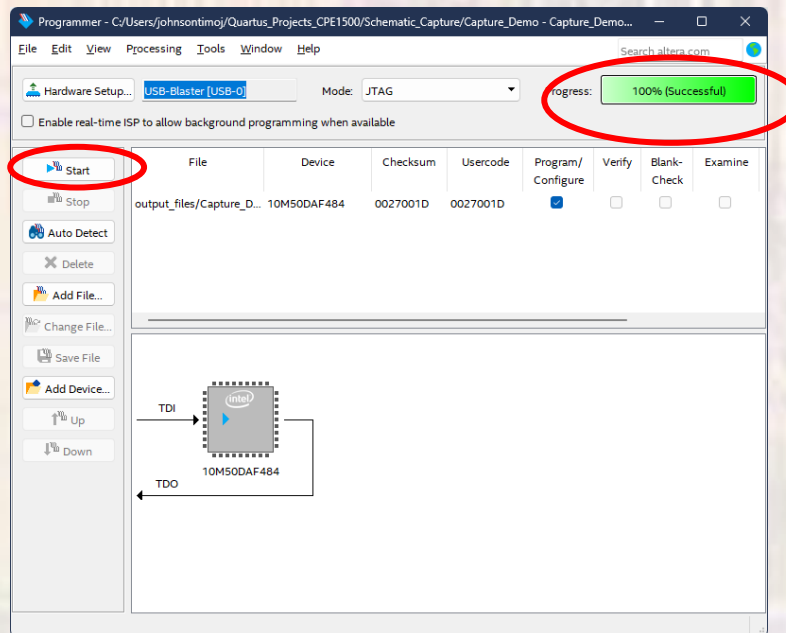
```
! 18236 Number of processors has not been specified which may cause overloading
! 10905 Generated the EDA functional simulation netlist because it is the only s
i 204019 Generated file Capture_Demo.vho in folder "C:/Users/johnsontimobj/Quartus
i Quartus Prime EDA Netlist Writer was successful. 0 errors, 3 warnings
i 293000 Quartus Prime Full Compilation was successful. 0 errors, 19 warnings
```



# Schematic to DE10

## 6) Download the design to the DE10

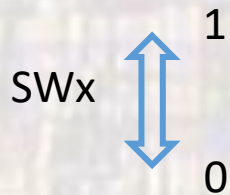
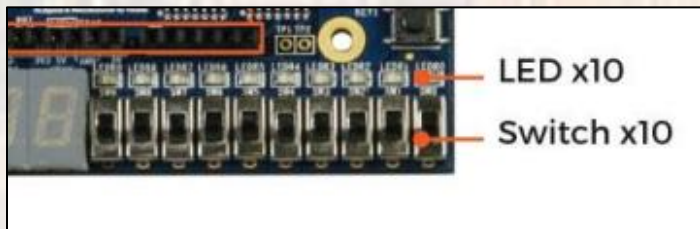
- Plug the DE10 board into your laptop USB port
  - Should be lots of flashing lights
- **Tools** → **Programmer**
  - The USB Blaster interface should have been setup when you setup Quartus – see Quartus Setup Slides if it is not visible
- **Start**



# Schematic to DE10

## 7) Verify the design

- Choose a value for SW1 and SW0 (SEL(1) and SEL(0))
- Verify only the associated SW(9-6) toggle the LED on/off



SEL1	SEL0	SW/LED OUT
0	0	Only SW 6 = 1 causes LED 5 to light
0	1	Only SW 7 = 1 causes LED 5 to light
1	0	Only SW 8 = 1 causes LED 5 to light
1	1	Only SW 9 = 1 causes LED 5 to light