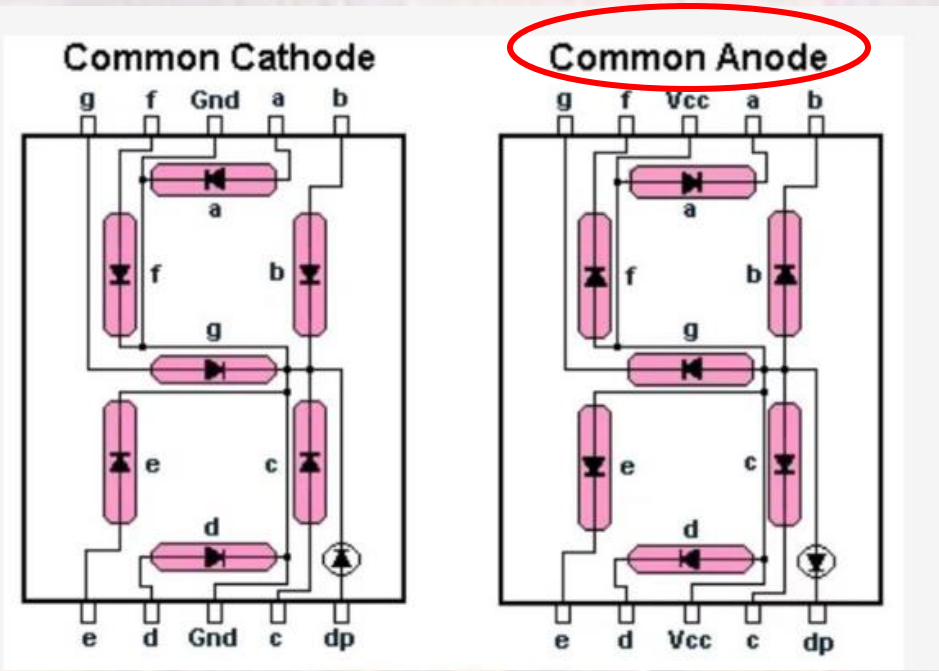
SSEG Display

- There are two standard 7-segment display variations
  - The DE10 uses the Common Anode variation
    - Pulling a pin LOW causes the LED to turn on



Typically wired as

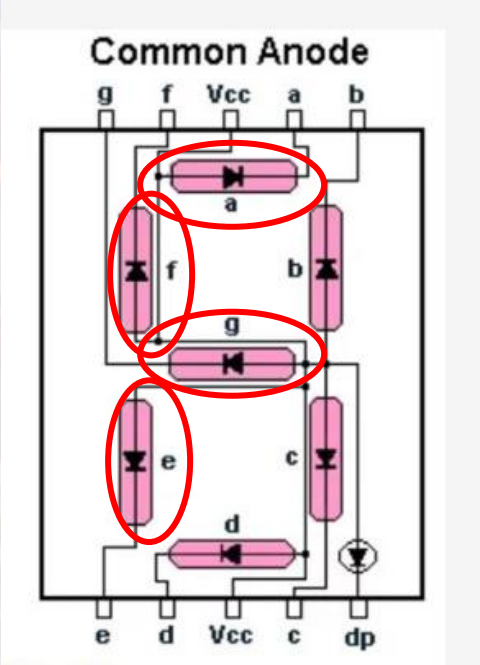
dp g f e d c b a

msb lsb

© tj

SSEG Display

- The DE10 uses the Common Anode variation
  - Active low to turn on the diodes



Display the letter F

dp	g	f	e	d	c	b	a
off	on	on	on	off	off	off	on

active low (DE10)

1	0	0	0	1	1	1	0

© tj

SSEG Display

- DE10 Code Example
  - The seven segment displays are called HEX0 – HEX5

in the port map:

```
o_sseg_out:        out   std_logic_vector(7 downto 0);
```

In the architecture

```
-- output the letter F
o_sseg_out <= 0x8E;
```

1 0 0 0 1 1 1 0

In the pin planner – map the pins

Signal Name	FPGA Pin No.	Description	I/O S
HEX30	PIN_F21	Seven Segment Digit 3[0]	3.3-V
HEX31	PIN_E22	Seven Segment Digit 3[1]	3.3-V
HEX32	PIN_E21	Seven Segment Digit 3[2]	3.3-V
HEX33	PIN_C19	Seven Segment Digit 3[3]	3.3-V
HEX34	PIN_C20	Seven Segment Digit 3[4]	3.3-V
HEX35	PIN_D19	Seven Segment Digit 3[5]	3.3-V
HEX36	PIN_E17	Seven Segment Digit 3[6]	3.3-V
HEX37	PIN_D22	Seven Segment Digit 3[7] , DP	3.3-V

Named: * Edit: PIN_C20 Filter: Pins: all

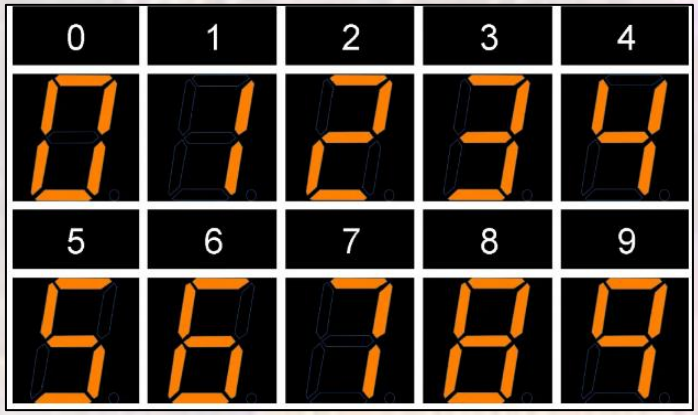
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Stanc
o_sseg_out[6]	Output				PIN_B4	2.5 V (defau
o_sseg_out[5]	Output				PIN_B5	2.5 V (defau
o_sseg_out[4]	Output	PIN_C20	6	B6_N0	PIN_F7	2.5 V (defau
o_sseg_out[3]	Output	PIN_C19	7	B7_N0	PIN_E8	2.5 V (defau
o_sseg_out[2]	Output				PIN_C5	2.5 V (defau
o_sseg_out[1]	Output				PIN_D5	2.5 V (defau
o_sseg_out[0]	Output				PIN_C4	2.5 V (defau

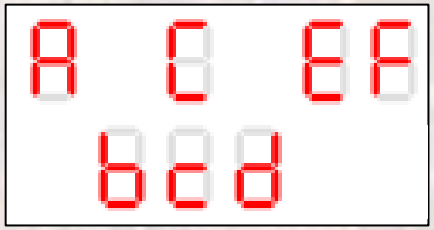
Mapped to HEX3

© tj

SSEG Display

- Hex Characters





- Full Alphabet