VHDL

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VHDL

- VHDL
- VHSIC Hardware Description Language
- Very High Speed Integrated Circuit

VHDL

$\boxed{\text{This is not a programming language}}$

VHDL

- Early Development
  - Department of Defense
  - 1983-1985 (first release)
  - IEEE standard version - 1987
  - Developed by committee
    - Many DOD contractors involved
  - 2 goals
    - Document Integrated Circuits
    - Simulate Integrated Circuits
    - Both goals allowed the DOD to move designs from one contractor to another contractor if needed

Note: No requirement for synthesis in the early development
VHDL contains many elements that are focused on documentation and design
These elements CANNOT be used to create logic

VHDL

- Advances
  - Private companies created tools to synthesize logic from the VHDL descriptions
    - Mentor Graphics
    - Synopsis
    - Cadence
    - Intel/Altera
    - Xylinx
  - Additional signal types and libraries were added
    - Multi-level logic, unknown
    - std_logic, signed, unsigned, …

Note: Once synthesis was introduced – the language was effectively broken into 2 parts
Synthesizable VHDL
Un-synthesizable VHDL

VHDL

- Synthesizable constructs
  - Code that can be converted to hardware
  - Concurrent logic
  - Sequential logic (processes with edge detection)
  - Structural code
  - with-select, when-else, …
  - if-else, case, …

- Un-synthesizable constructs
  - Code that cannot be converted to hardware
    - Allowed for simulation, descriptive or compilation purposes
  - Time – wait, delay
  - Loops – while, for, …
  - Initial conditions
  - Variables
    - Strictly speaking variables can be used in synthesis – but it is very dangerous – and we will not do it!

VHDL

- Major Releases
  - 1985 – baseline
  - 1987 – first IEEE release
  - 1994
  - 2000
  - 2002
  - 2009 – called VHDL 2008

Note: Most – but not all – tools now support the 2008 version