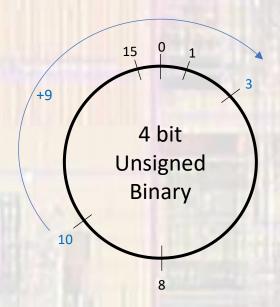
Last updated 1/7/25

- Unsigned Addition
 - Overflow Interpretation

4 bit
Unsigned Binary
Number Line



Overflow

19 does not fit in 4 bit unsigned

Result in 4 bits is 3

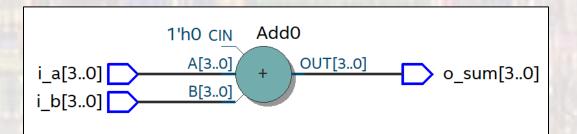
- Unsigned Addition
 - I/Os must be converted to/from unsigned to allow addition

```
adder_4bit_unsigned.vhdl
    by: johnsontimoi
    created: 12/31/24
    version: 0.0
    4bit unsigned adder
    inputs: a, b
    outputs: sum
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity adder_4bit_unsigned is
                          in std_logic_vector(3 downto 0);
in std_logic_vector(3 downto 0);
   port( i_a:
          i_b:
                          out std_logic_vector(3 downto 0)
          o sum:
end entity;
```

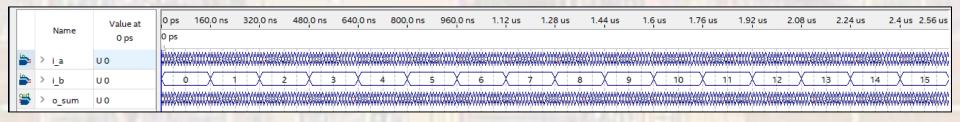
```
architecture behavioral of adder_4bit_unsigned is
  signal a_sig: unsigned(3 downto 0);
  signal b_sig: unsigned(3 downto 0);
  signal sum_sig: unsigned(3 downto 0);

begin
  a_sig <= unsigned(i_a);
  b_sig <= unsigned(i_b);
  sum_sig <= a_sig + b_sig;
  o_sum <= std_logic_vector(sum_sig);
end architecture;</pre>
```

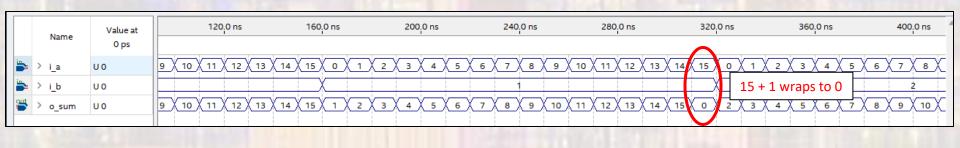
Unsigned Addition



Flow Summary	
< <filter>></filter>	
Flow Status	Successful - Tue Jan 07 17:16:56 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	adder_4bit_unsigned
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	4
Total registers	0
Total pins	12
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



- Unsigned Addition
 - Wrapping on overflow



	Name	Value at	ns	76	0,0 ns			800 _. 0 ns			840.	0 ns			880,0) ns			920.0	ns			960.0 ns		1.0 us		1.04 u 4
	0 ps																										
<u> </u>	> i_a	UO	8 X 9	X 10 X 11	12	13	14	15 0	X 1	2	3	4	5	6	7 X	8 X	9	10	11	12 X	13	14 X	15 🗸 0	1 × 2 ×	3 4	5 (6)	7
<u> </u>	> i_b	UO													5								13 + 5	wraps to	2		6
*	> o_sum	UO	2 13	14 15	X o	1	2	3 \ 5	6	7	8	9	10	11	12	13	14	15	• X	1	2	3	4 (6)	7 8	9 10	11 12	13 1

_											
	Name	Value at	IS	2.04 us	2.08 us	2.12 us	2.16 us	2.2 us	2.24 us	2.28 us	2.32
	Name	0 ps									
	ъ > i_a	UO	8 X 9 X	10 11 12 13	14 15 0 1	2 3 4 5	6 7 8 9	10 11 12 1	3 \ 14 \ 15 \ 0 \ 1 \ 2	3 4 5	6 X 7 X
	> i_b	UO			X		13		11 + 13 wraps to 8		14
9	> o_sum	UO	4 X 5 X	6 X 7 X 8 X 9 X	10 11 13 14	15 X 0 X 1 X 2 X	3 4 5 6	7 8 9 10	0 X 11 X 12 X 14 X 15 X 0	X 1 X 2 X 3	4 X 5 X

- Signed Addition
 - Overflow Interpretation

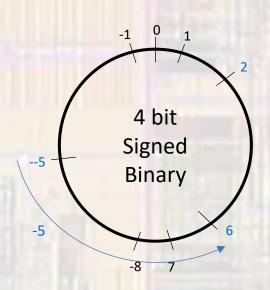
4 bit signed binary

Overflow

MSB Carry-out ≠ carry-in

Result in 4 bits is 6

4 bit Signed Binary Number Line



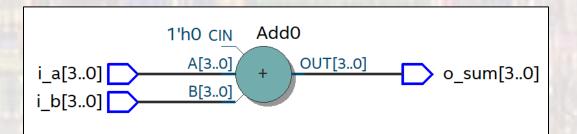
- Signed Addition
 - I/Os must be converted to/from signed to allow addition

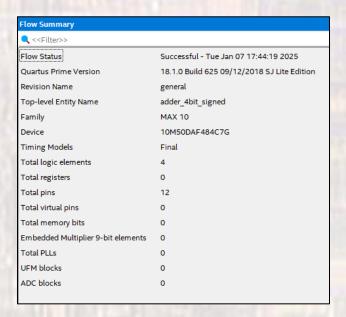
```
adder_4bit_signed.vhdl
   by: johnsontimoj
   created: 12/31/24
   version: 0.0
   4bit signed adder
   inputs: a, b
   outputs: sum
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all:
entity adder_4bit_signed is
  end entity:
```

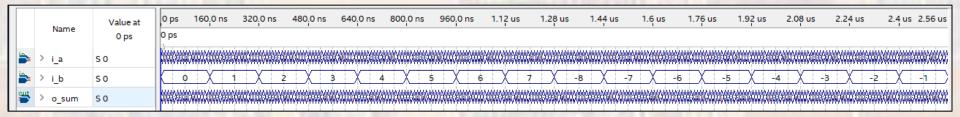
```
architecture behavioral of adder_4bit_signed is
  signal a_sig: signed(3 downto 0);
  signal b_sig: signed(3 downto 0);
  signal sum_sig: signed(3 downto 0);

begin
  a_sig <= signed(i_a);
  b_sig <= signed(i_b);
  sum_sig <= a_sig + b_sig;
  o_sum <= std_logic_vector(sum_sig);
end architecture;</pre>
```

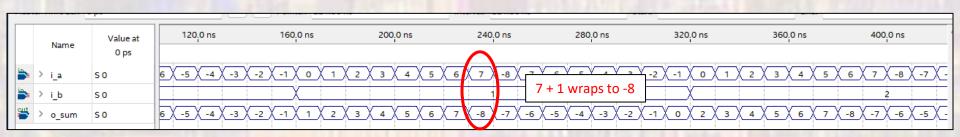
Signed Addition







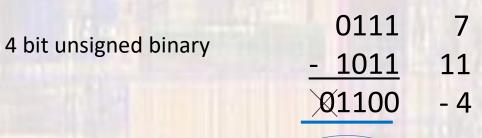
- Signed Addition
 - Wrapping on overflow



	N	Value at	760,0 ns	800,0 ns	840,0 ns	880.0 ns	920,0 ns	960 _. 0 ns	1.0 us	1.04 us
	Name	0 ps								
in	≥	S 0	6 \ -5 \ -4 \ -3 \	-2 X -1 X 0 X 1 X	2 3 4 5	6 X 7 X -8 X -7	-6 X -5 X -4 X -3	(-2 \\ -1 \\ 0 \\ 1 \\	2 × 3 × 4 × 5	6 7 -8 -7 -
in	≥	S 0		X		5 5+	5 wraps to -6	X		6
4	> o_sum	S 0	2 X -1 X 0 X 1 X	2 X 3 X 5 X 6 X	7 \(-8 \) -7 \(-6 \)	-5 \ -4 \ -3 \ \ -2 \	<u>-1 </u>	3 4 6 7 7 -	8 (-7 (-6 (-5	-4 \ -3 \ \ -2 \ \ -1 \ \

1				_							
	Nesse	Value at	8 us	1.72 us	1.76 us	1.8 us	1.84 us	1.88 us	1.92 us	1.96 us	2. '
	Name	0 ps									
<u> </u>	: > i_a	S 0	X-8 X-7 X-6	6 \ -5 \ -4 \ -3 \ -	2 X -1 X 0 X 1 X	2 3 4 5	6 7 -8 -7 -6	-5 \ -4 \ \ -3	-2 X -1 X 0 X 1 X	2 X 3 X 4 X 5 X 6	7
<u> </u>	> i_b	S 0	-6		\square X		-5	-	5 + -5 wraps to 6		
=	o_sum	S 0	2 3 4	4 × 5 × 6 × 7 × -	8 \ -7 \ -5 \ -4 \	-3 \ -2 \ -1 \ 0	1 2 3 4 5	6 X 7 X -8	-7 <u>X -6 X -4 X -3 X -</u>	2 X -1 X 0 X 1 X 2	3

- Unsigned Subtraction
 - Wrapping Interpretation

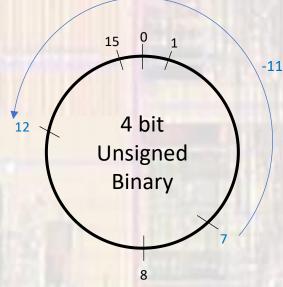


Wrap

-4 does not exist in 4 bit unsigned

Result in 4 bits is 12

4 bit
Unsigned Binary
Number Line

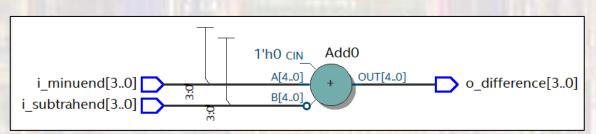


- Unsigned Subtraction
 - I/Os must be converted to/from unsigned to allow subtraction

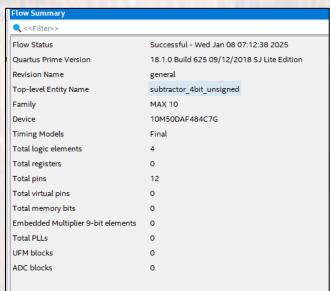
```
subtractor_4bit_unsigned.vhdl
    by: johnsontimoj
    created: 12/31/24
    version: 0.0
    4bit unsigned subtractor
    inputs: minuend, subtrahend
    outputs: difference
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity subtractor_4bit_unsigned is
                             in std_logic_vector(3 downto 0);
in std_logic_vector(3 downto 0);
   port( i_minuend:
         i subtrahend:
         o_difference:
                             out std_logic_vector(3 downto 0)
end entity:
```

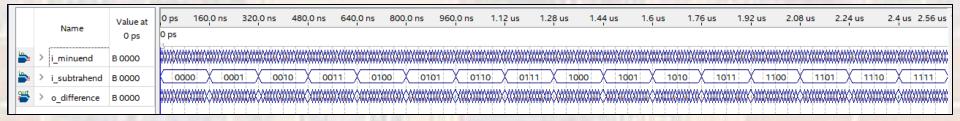
```
architecture behavioral of subtractor_4bit_unsigned is
                               unsigned(3 downto 0);
            minuend_sig:
   signal
            subtrahend_sig:
                               unsigned(3 downto 0);
   signal
            difference_sig:
                               unsigned(3 downto 0):
   signal
begin
   minuend_sig <= unsigned(i_minuend);
   subtrahend_sig <= unsigned(i_subtrahend);
   difference_sig <= minuend_sig - subtrahend_sig:</pre>
   o_difference <= std_logic_vector(difference_sig);</pre>
end architecture;
```

Unsigned Subtraction

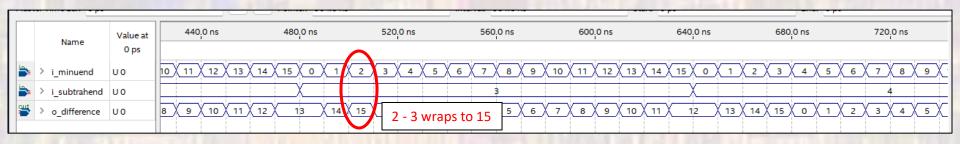


Note – this is not an obvious model more info in ELE3510





- Unsigned Subtraction
 - Wrapping



	Name	Value at	1.24 us	1.28 us	1.32 us		1.36 us	1.4 us	1.44 us	1.48 us	1.52 us
		0 ps									
-	i_minuend	U O	11 12 13 14	X 15 X 0 X 1 X 2	2 X 3 X 4	5 6	7 8 9	10 11 12 13	14 15 0 1	2 3 4 5	6 7 8 9 10
=	i_subtrahend	UO					8		X		9
==	> o_difference	UO	4	X 8 X 9 X 1	0 X 11 X 12	13 14	5 – 8 wraps	to 13 × 4 × 5	6	9 X 10 X 11 X 12 X	13 X 14 X 15 X 0 X 1

		Value at	us	1.88 us	1.92 us	1.96 us	2.0 us	2.04 us	2.08 us	2.12 us	2.16
	Name	0 ps									
<u> </u>	i_minuend	U O	8	9 10 11 12 13 14	1 15 0 1	2 3 4 5	6 7 8 9	10 11 12 13	14 15 0 1	2 3 4 5	6 X 7
<u> </u>	i_subtrahend	UO	1		X		12		X		1
=	> o_difference	UO	13 🗡 1	14 15 0 1 2 3	4 (5)	6 X 7 X 8 X 9 X	6 - 12 wra	aps to 10	2 3 4	5 X 6 X 7 X 8 X	9 (10)