VHDL
Adders / Subtractors

Last updated 1/7/25

VHDL Adders/Subtractors

- Unsigned Addition
  - Overflow – Interpretation

4 bit unsigned binary

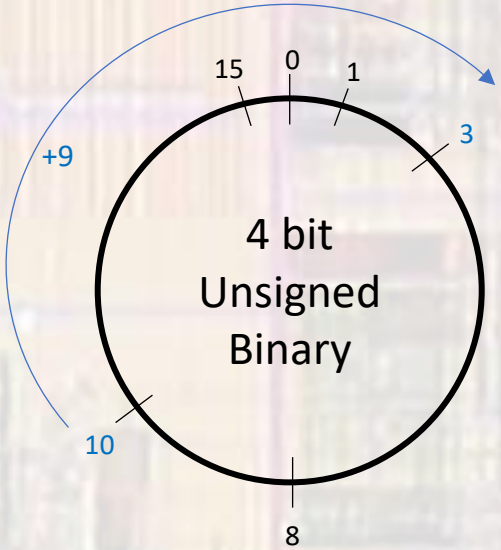
```
  1 0 0 0
    1010   10
+   1001    9
  ~10011~  19
```

Overflow

19 does not fit in 4 bit unsigned

Result in 4 bits is 3

4 bit
Unsigned Binary
Number Line



VHDL Adders/Subtractors

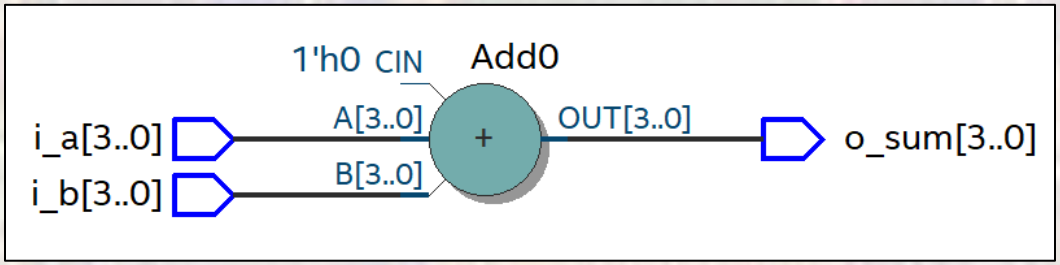
- Unsigned Addition
  - I/Os must be converted to/from unsigned to allow addition

```
----------------------------------
--
--  adder_4bit_unsigned.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  4bit unsigned adder
--
--  inputs: a, b
--
--  outputs: sum
--
----------------------------------
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity adder_4bit_unsigned is
   port( i_a:           in std_logic_vector(3 downto 0);
         i_b:           in std_logic_vector(3 downto 0);
         o_sum:         out std_logic_vector(3 downto 0)
   );
end entity;
```

```
architecture behavioral of adder_4bit_unsigned is

   signal   a_sig:   unsigned(3 downto 0);
   signal   b_sig:   unsigned(3 downto 0);
   signal   sum_sig: unsigned(3 downto 0);

begin

   a_sig <= unsigned(i_a);
   b_sig <= unsigned(i_b);

   sum_sig <= a_sig + b_sig;

   o_sum <= std_logic_vector(sum_sig);

end architecture;
```

VHDL Adders/Subtractors

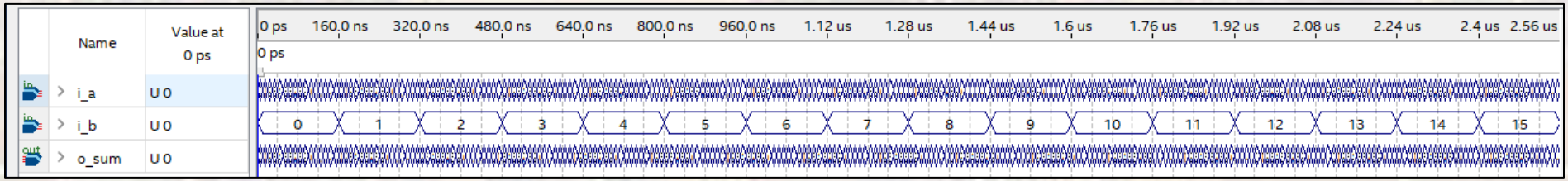
- Unsigned Addition



Flow Summary

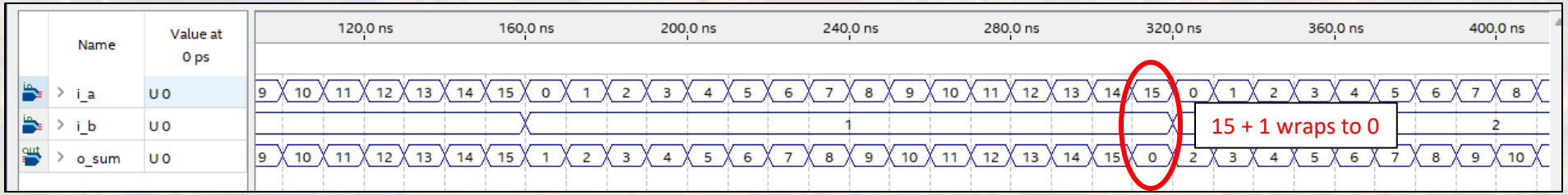
<<Filter>>

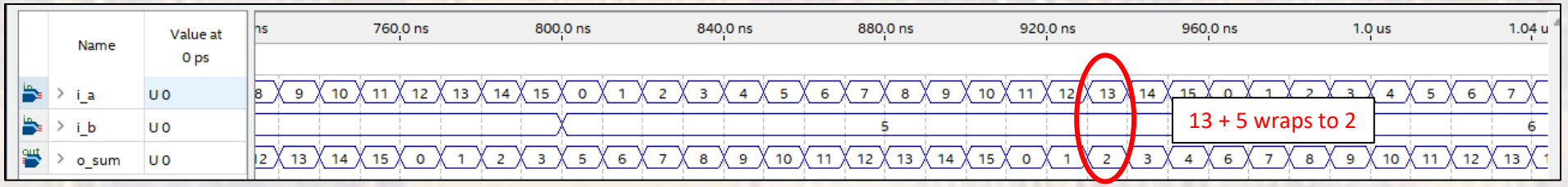
Flow Status	Successful - Tue Jan 07 17:16:56 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	adder_4bit_unsigned
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	4
Total registers	0
Total pins	12
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

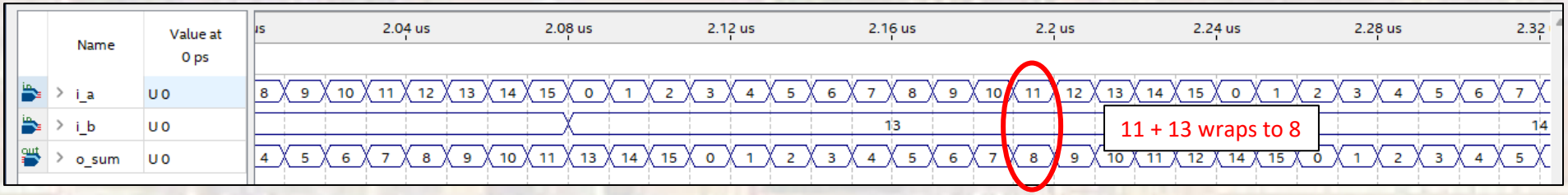


VHDL Adders/Subtractors

- Unsigned Addition
  - Wrapping on overflow







VHDL Adders/Subtractors

- Signed Addition
  - Overflow – Interpretation

4 bit signed binary

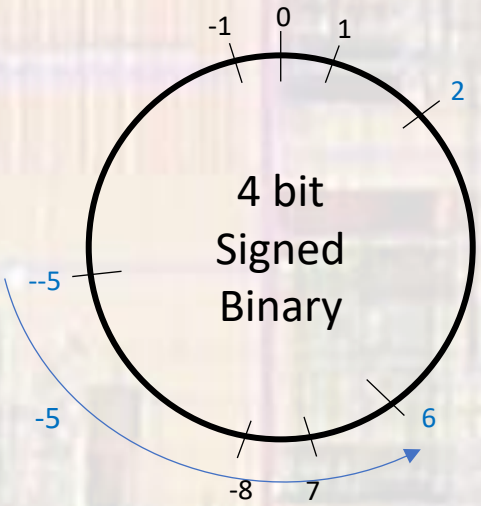
```
  1 0 1 1
    1011   - 5
+   1011   - 5
  ~~1~~0110  -10
```

Overflow

MSB Carry-out ≠ carry-in

Result in 4 bits is 6

4 bit
Signed Binary
Number Line



VHDL Adders/Subtractors

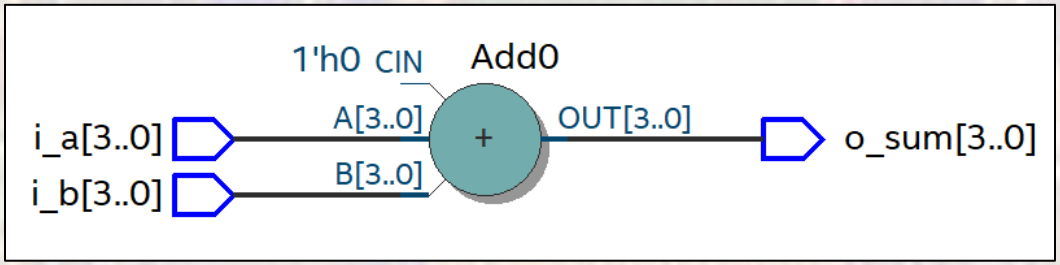
- Signed Addition
  - I/Os must be converted to/from signed to allow addition

```
----------------------------------
--
--  adder_4bit_signed.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  4bit signed adder
--
--  inputs: a, b
--
--  outputs: sum
--
----------------------------------
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity adder_4bit_signed is
   port( i_a:           in std_logic_vector(3 downto 0);
         i_b:           in std_logic_vector(3 downto 0);
         o_sum:         out std_logic_vector(3 downto 0)
   );
end entity;
```

```
architecture behavioral of adder_4bit_signed is

   signal   a_sig:   signed(3 downto 0);
   signal   b_sig:   signed(3 downto 0);
   signal   sum_sig: signed(3 downto 0);

begin

   a_sig <= signed(i_a);
   b_sig <= signed(i_b);

   sum_sig <= a_sig + b_sig;

   o_sum <= std_logic_vector(sum_sig);

end architecture;
```

VHDL Adders/Subtractors

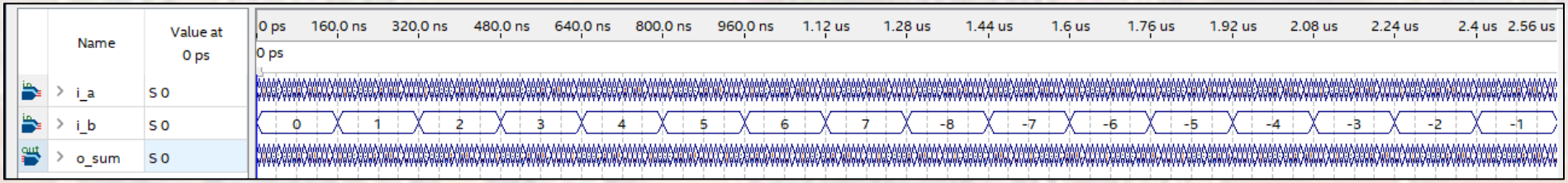
- Signed Addition



Flow Summary

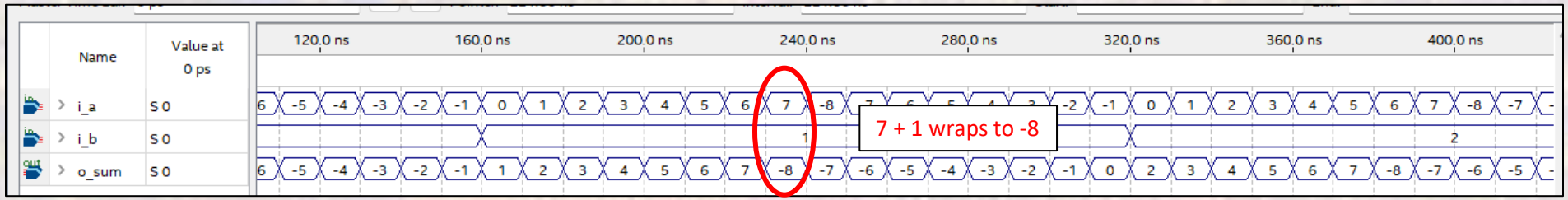
<<Filter>>

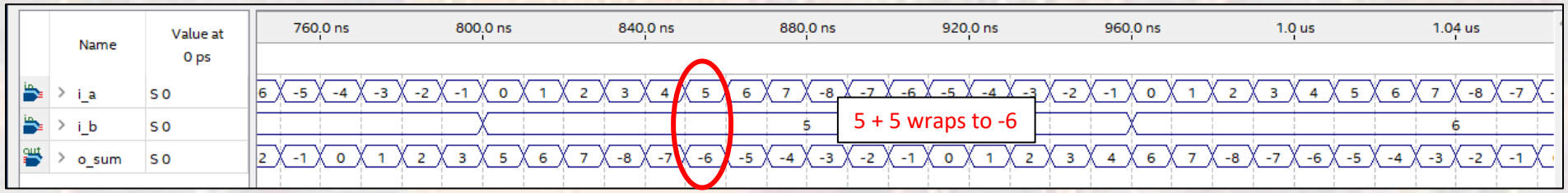
Flow Status	Successful - Tue Jan 07 17:44:19 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	adder_4bit_signed
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	4
Total registers	0
Total pins	12
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

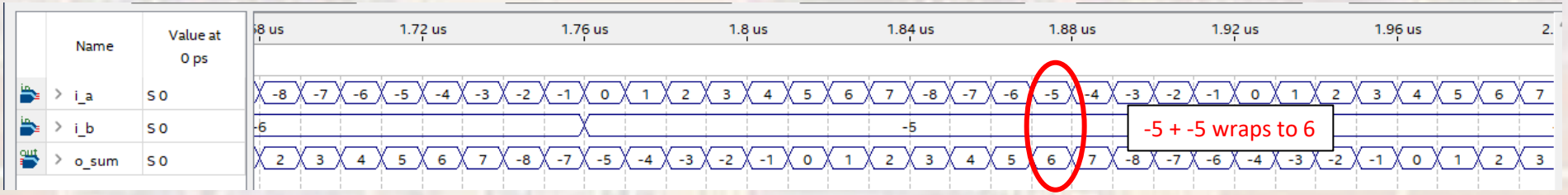


VHDL Adders/Subtractors

- Signed Addition
  - Wrapping on overflow







VHDL Adders/Subtractors

- Unsigned Subtraction
  - Wrapping – Interpretation

4 bit unsigned binary

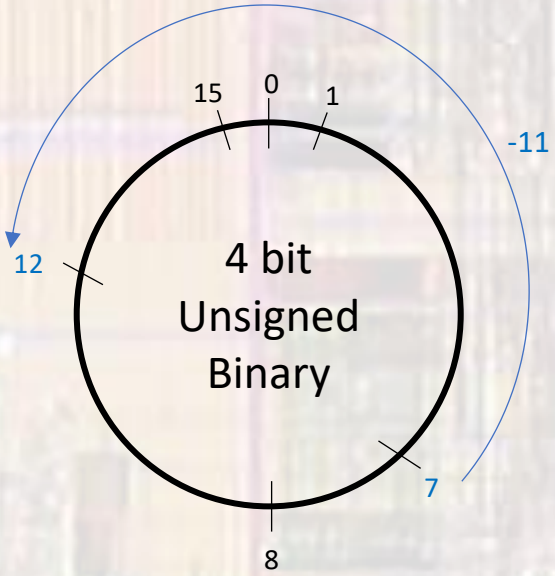
	0111	7
-	1011	11
	~~0~~1100	- 4

Wrap

-4 does not exist in 4 bit unsigned

Result in 4 bits is 12

4 bit
Unsigned Binary
Number Line



VHDL Adders/Subtractors

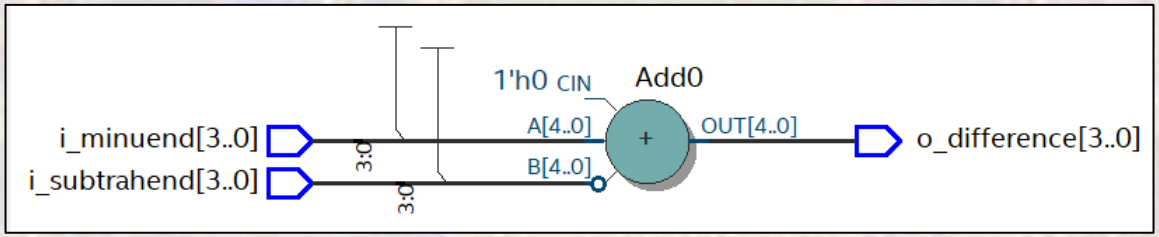
- Unsigned Subtraction
  - I/Os must be converted to/from unsigned to allow subtraction

```
----------------------------------
--
--  subtractor_4bit_unsigned.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  4bit unsigned subtractor
--
--  inputs: minuend, subtrahend
--
--  outputs: difference
--
----------------------------------
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity subtractor_4bit_unsigned is
   port( i_minuend:         in std_logic_vector(3 downto 0);
         i_subtrahend:      in std_logic_vector(3 downto 0);
         o_difference:      out std_logic_vector(3 downto 0)
   );
end entity;
```

```
architecture behavioral of subtractor_4bit_unsigned is

   signal   minuend_sig:      unsigned(3 downto 0);
   signal   subtrahend_sig:   unsigned(3 downto 0);
   signal   difference_sig:   unsigned(3 downto 0);

begin

   minuend_sig <= unsigned(i_minuend);
   subtrahend_sig <= unsigned(i_subtrahend);

   difference_sig <= minuend_sig - subtrahend_sig;

   o_difference <= std_logic_vector(difference_sig);

end architecture;
```

VHDL Adders/Subtractors

- Unsigned Subtraction

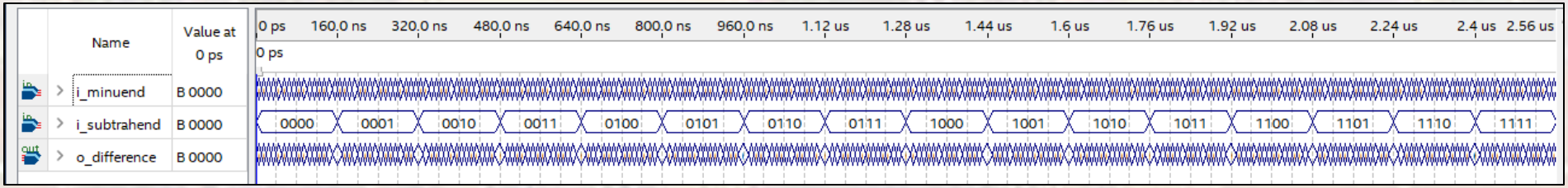


Note – this is not an obvious model
more info in ELE3510

Flow Summary

<<Filter>>

Flow Status	Successful - Wed Jan 08 07:12:38 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	subtractor_4bit_unsigned
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	4
Total registers	0
Total pins	12
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



VHDL Adders/Subtractors

- Unsigned Subtraction
  - Wrapping