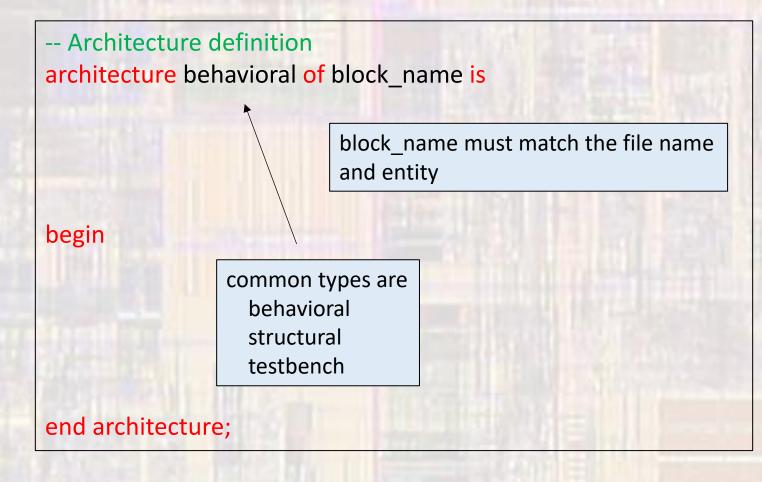
## Last updated 1/1/25

- The VHDL architecture is the description of the block's functionality
  - Type
    - Identifies the kind of architecture described
    - User defined: Common types:
      - behavioral
      - structural
      - testbench
  - Declarations
    - Internal signal declarations
    - Included hierarchical block descriptions
  - Functional Description
    - Logic operations
    - Instantiated blocks with connections

Format - Block



### Format - Declarations

```
-- Architecture definition
architecture behavioral of block_name is
signal sig_name1 std_logic; declare any internal signals
signal sig_name2 std_logic_vector(7 downto 0);
```

```
component component_name is
```

generic(...

```
port(...
);
end component;
```

begin

```
end architecture;
```

component description for any structural elements – matches the entity for that component

### Format – Definitions / Instantiations

```
-- Architecture definition
architecture behavioral of block_name is
begin
    sigZ <= sigX OR sigY;
    sigC \le sigA when sigD = '0' else
                                              behavioral / logic descriptions
            sigB when sigD = (1');
    inst_0: component_name
       generic map( ...
                                    instantiation of any structural blocks
       port map(...
                 );
end architecture;
```

### Example

### Declarations

architecture logic of oddeven\_16bit\_logic\_structural is

#### -- internal signals signal sig\_15\_12: std\_logic; signal sig\_11\_8: std\_logic; signal sig\_7\_4: std\_logic; signal sig\_3\_0: std\_logic; component oddeven\_4bit\_logic is port( i\_a: in std\_logic; i\_b: in std\_logic; i\_c: in std\_logic; i\_d: in std\_logic; o\_oddeven\_out: out std\_logic );

end component;

### **Definitions / Instantiations**

#### begin oe\_1512: oddeven\_4bit\_logic port map( i\_a => i\_in(15), i\_b => i\_in(14), => i\_in(13), i\_c i\_d => i\_in(12), o\_oddeven\_out => sig\_15\_12 ); oe\_1108: oddeven\_4bit\_logic => i\_in(11), port map( i\_a i\_b $=> i_i(10),$ => i\_in(9), i\_c i\_d $=> i_i(8)$ , o\_oddeven\_out => sig\_11\_8 ); oe\_0704: oddeven\_4bit\_logic port map( i\_a => i\_in(7), i\_b $=> i_{i_{(6)}}$ => i\_in(5), i\_c => i\_in(4), id o\_oddeven\_out => sig\_7\_4 ); oe\_0300: oddeven\_4bit\_logic port map( $=> i_i(3),$ i\_a i\_b $=> i_i(2),$ => i\_in(1), i\_c i\_d $=> i_i(0),$ o\_oddeven\_out => sig\_3\_0 ): oe\_final: oddeven\_4bit\_logic port map( i\_a => NOT sig\_15\_12, => NOT sig\_11\_8, i\_b $\Rightarrow$ NOT sig\_7\_4, i\_c i\_d => NOT sig\_3\_0, o\_oddeven\_out => o\_oddeven\_out ); end architecture;

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