

VHDL Comparators

Last updated 1/8/25

VHDL Comparators

- Vector Comparison
 - `std_logic_vector`
 - Does not have a numeric interpretation
 - Only 'safe' comparison operators
 - `=`
 - `/=`
 - `signed`, `unsigned`
 - Do have numeric interpretations
 - Comparison operators
 - `=`
 - `/=`
 - `>`
 - `<`
 - `>=`
 - `<=`

VHDL Comparators

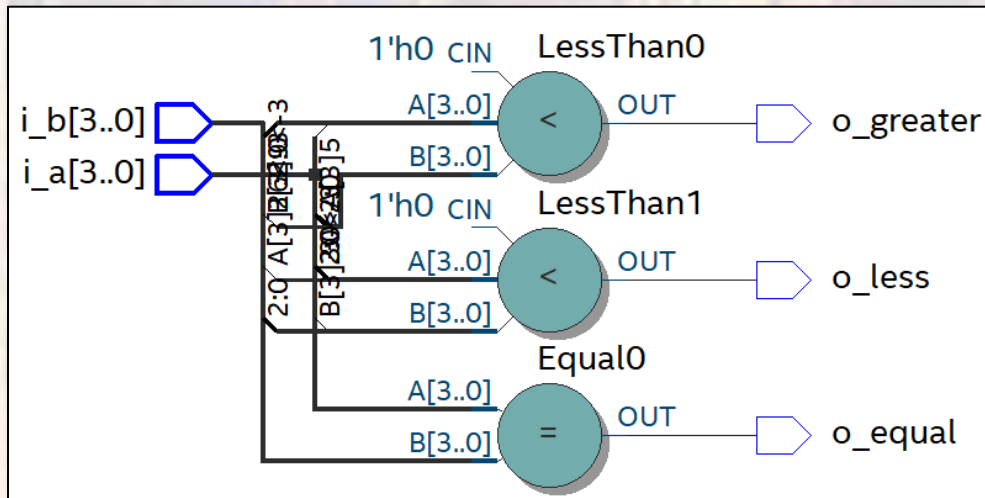
- Signed Comparison
 - I/Os must be converted to/from signed to allow comparison

```
-----  
-- comparator_3way_4bit_signed.vhdl  
-- by: johnsontimoj  
-- created: 12/31/24  
-- version: 0.0  
-----  
-- 4bit 3way comparator  
-- inputs: a, b  
-- outputs: greater, equal, less  
-----  
library IEEE;  
use ieee.std_logic_1164.all;  
use ieee.numeric_std.all;  
  
entity comparator_3way_4bit_signed is  
  port( i_a:      in std_logic_vector(3 downto 0);  
        i_b:      in std_logic_vector(3 downto 0);  
        o_greater: out std_logic;  
        o_equal:  out std_logic;  
        o_less:   out std_logic  
  );  
end entity;
```

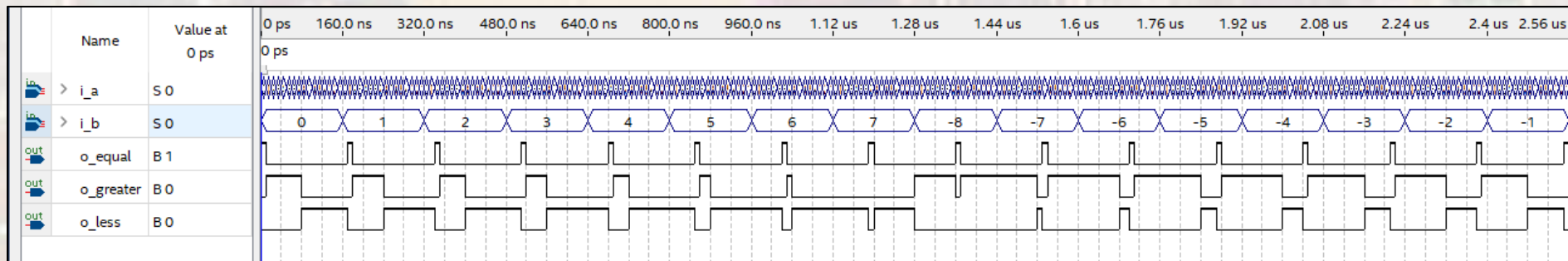
```
architecture behavioral of comparator_3way_4bit_signed is  
  signal a_sig: signed(3 downto 0);  
  signal b_sig: signed(3 downto 0);  
  
begin  
  a_sig <= signed(i_a);  
  b_sig <= signed(i_b);  
  
  o_greater <= '1' when a_sig > b_sig else '0';  
  o_equal   <= '1' when a_sig = b_sig else '0';  
  o_less    <= '1' when a_sig < b_sig else '0';  
  
end architecture;
```

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- Signed Comparison



Flow Summary	
Filter	
Flow Status	Successful - Wed Jan 08 09:05:08 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	comparator_3way_4bit_signed
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	9
Total registers	0
Total pins	11
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



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