# VHDL Counters

Last updated 1/9/25

# VHDL Counters

- Counters
  - Used as individual blocks
  - Used inside a block
    - Timers – delays, time-out, …
    - Collectors – cash, presses, …
  - Variations
    - Up, Down, Up-Down
    - Wrapping, non-wrapping
    - Modulo
    - Fixed size, n-bit
    - Fixed increment, m-increment

  - Use signed or unsigned signals to allow addition and subtraction

# VHDL Counters

- Counter – up - 4 bit - unsigned

```
----------------------------------
--
--  counter_up_unsigned_4bit.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  standard 4 bit up counter using unsigned
--  inputs: clk, rstb,
--
--  outputs: cnt
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity counter_up_unsigned_4bit is
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;

      o_cnt :   out std_logic_vector(3 downto 0)
   );
end entity;
```

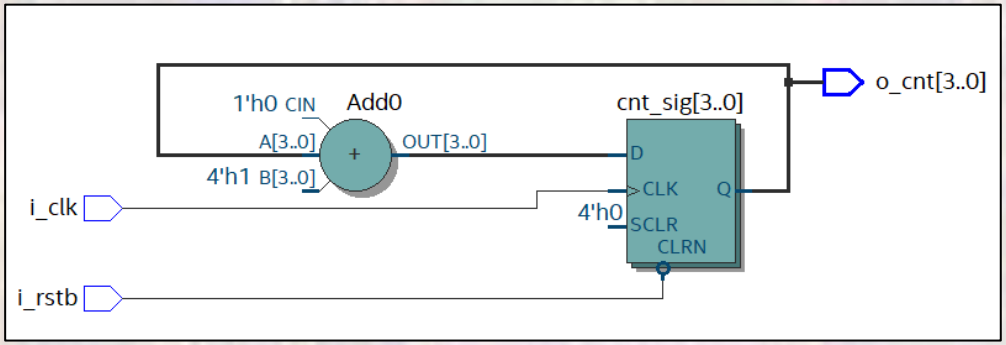
```
architecture behavioral of counter_up_unsigned_4bit is

   signal cnt_sig:   unsigned(3 downto 0);

begin

   process (i_clk, i_rstb)
   begin
      -- asynch
      if (i_rstb = '0') then
         cnt_sig <= "0000";
      -- synch
      elsif (rising_edge(i_clk)) then
         cnt_sig <= cnt_sig + 1;
      end if;          -- main - no else needed - FF template being used
   end process;

   o_cnt <= std_logic_vector(cnt_sig);

end architecture;
```

needed for addition

cast

# VHDL Counters

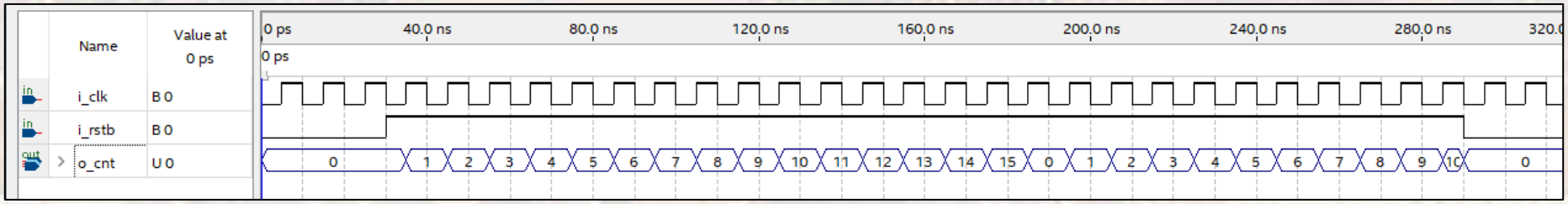
- Counter – up - 4 bit - unsigned




**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | Successful - Thu Jan 09 15:04:34 2025 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | general |
| Top-level Entity Name | counter_up_unsigned_4bit |
| Family | MAX 10 |
| Device | 10M50DAF484C7G |
| Timing Models | Final |
| Total logic elements | 4 |
| Total registers | 4 |
| Total pins | 6 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |
| UFM blocks | 0 |
| ADC blocks | 0 |




reset | counting up | roll over | reset

# VHDL Counters

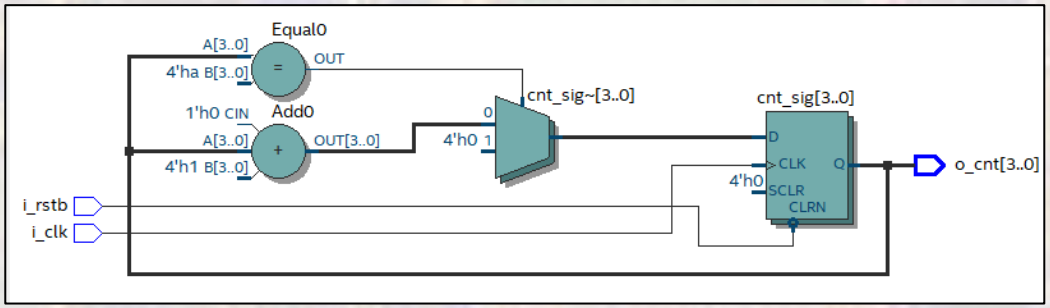
- Counter – up – mod11

```
----------------------------------
--
--  counter_up_mod11.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  mod 11 up counter using unsigned
--  fixed to 4 bits due to mod 11
--
--  inputs: clk, rstb,
--
--  outputs: cnt
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity counter_up_mod11 is
   generic(
            MODVAL:  positive := 11
          );
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;

      o_cnt :   out std_logic_vector(3 downto 0)
   );
end entity;
```

```
architecture behavioral of counter_up_mod11 is

   signal cnt_sig:   unsigned(3 downto 0);

begin

   process (i_clk, i_rstb)
   begin
      -- asynch
      if (i_rstb = '0') then
         cnt_sig <= "0000";
      -- synch
      elsif (rising_edge(i_clk)) then
         -- check if current count is the max (MODVAL - 1)
         if(cnt_sig = (MODVAL - 1)) then
            cnt_sig <= "0000";
         else
            cnt_sig <= cnt_sig + 1;
         end if;  -- mod check
      end if;     -- main - no else needed - FF template being used
   end process;

   o_cnt <= std_logic_vector(cnt_sig);

end architecture;
```

# VHDL Counters

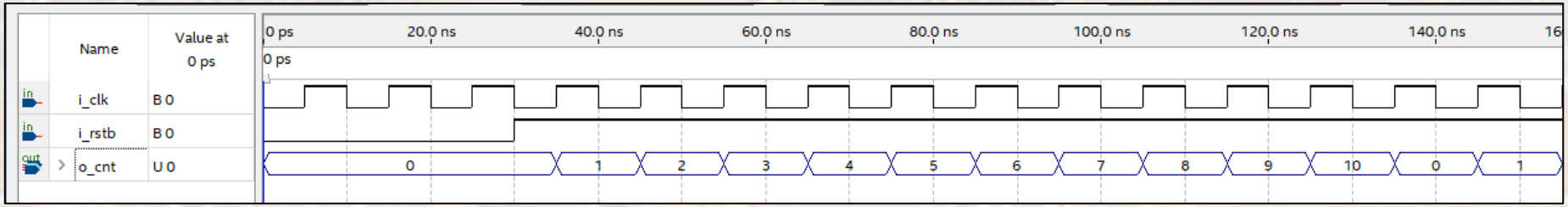
- Counter – up – mod11




**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | Successful - Thu Jan 09 15:22:22 2025 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | general |
| Top-level Entity Name | counter_up_mod11 |
| Family | MAX 10 |
| Device | 10M50DAF484C7G |
| Timing Models | Final |
| Total logic elements | 4 |
| Total registers | 4 |
| Total pins | 6 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |
| UFM blocks | 0 |
| ADC blocks | 0 |




reset

counting up

roll over

# VHDL Counters

- Counter – updown – signed - nbit

```
--
--  counter_updown_signed_nbit.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  signed nbit updown counter
--
--  inputs: clk, rstb, dir
--                      dir = 1 -> up
--
--  outputs: cnt
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity counter_updown_signed_nbit is
   generic(
            N: positive := 8
          );
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;
      i_dir:   in std_logic;

      o_cnt:   out std_logic_vector((N - 1) downto 0)
   );
end entity;
```

```
architecture behavioral of counter_updown_signed_nbit is

   signal cnt_sig:   signed((N - 1) downto 0);

begin

   process (i_clk, i_rstb)
   begin
      -- asynch
      if (i_rstb = '0') then
         cnt_sig <= (others => '0');
      -- synch
      elsif (rising_edge(i_clk)) then
         -- check dir
         if(i_dir = '1') then
            cnt_sig <= cnt_sig + 1;
         else
            cnt_sig <= cnt_sig - 1;
         end if;  -- dir check
      end if;     -- main - no else needed - FF template being used
   end process;

   o_cnt <= std_logic_vector(cnt_sig);

end architecture;
```

# VHDL Counters

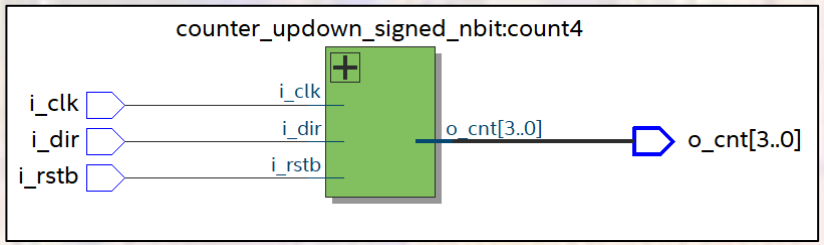
- Counter – updown – signed – nbit
  - 4 bit structural version

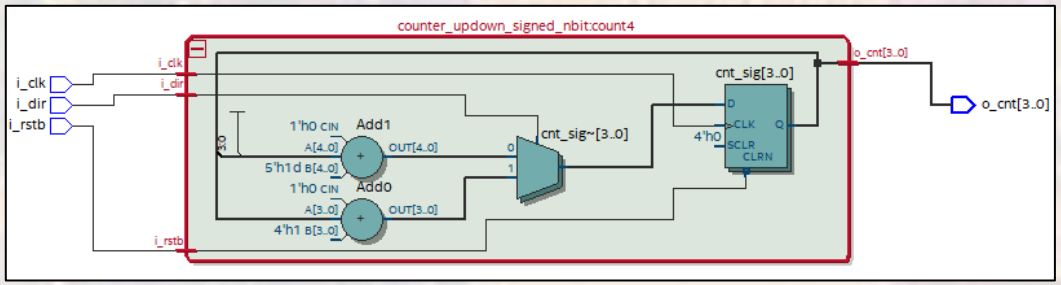
```
----------------------------------
--
--  counter_updown_signed_4bit_structural.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  signed 4bit updown counter structural
--
--  inputs: clk, rstb, dir
--                      dir = 1 -> up
--
--  outputs: cnt
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity counter_updown_signed_4bit_structural is
   generic(
            N: positive := 4
          );
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;
      i_dir:   in std_logic;

      o_cnt:   out std_logic_vector((N - 1) downto 0)
   );
end entity;
```

```
architecture structural of counter_updown_signed_4bit_structural is

   component counter_updown_signed_nbit is
      generic(
               N: positive := 8
             );
      port(
         i_clk:   in std_logic;
         i_rstb:  in std_logic;
         i_dir:   in std_logic;

         o_cnt:   out std_logic_vector((N - 1) downto 0)
      );
   end component;

begin

   count4: counter_updown_signed_nbit
   generic map( N => N
              )
   port map(   i_clk    => i_clk ,
               i_rstb   => i_rstb,
               i_dir    => i_dir,
               o_cnt    => o_cnt
            );

end architecture;
```

# VHDL Counters

- Counter – updown – signed – nbit
  - 4 bit structural version




| Flow Summary | |
|---|---|
| <<Filter>> | |
| Flow Status | Successful - Thu Jan 09 15:54:19 2025 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | general |
| Top-level Entity Name | counter_updown_signed_4bit_structural |
| Family | MAX 10 |
| Device | 10M50DAF484C7G |
| Timing Models | Final |
| Total logic elements | 5 |
| Total registers | 4 |
| Total pins | 7 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |
| UFM blocks | 0 |
| ADC blocks | 0 |