VHDL Decoders

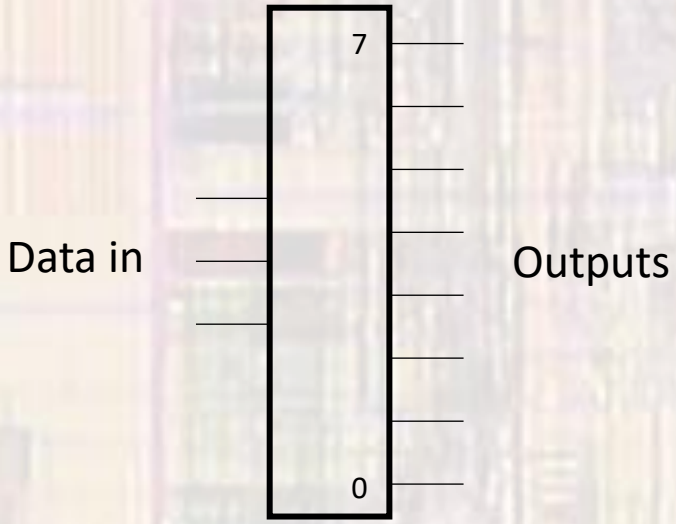
Last updated 1/1/25

VHDL Decoders

- A decoder sets one of many outputs to 1 based on the inputs
  - N data outputs – typically a power of 2
  - D data inputs – $\log_2(N)$
  - D:N Decoder

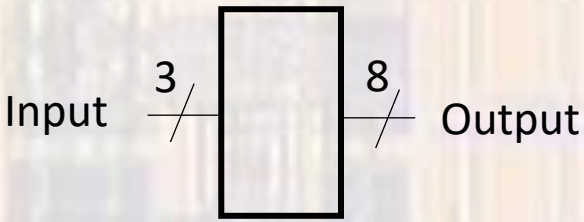
D = 3

N = 8



VHDL Decoders

- 3-8 Example
  - Description
  - Libraries
  - Entity




```
----------------------------------------
--
-- decoder_1.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
----------------------------------------
--
-- vhdl encoder example 1 - brute-force
--
----------------------------------------
--
-- Inputs: in(2-0)
-- Outputs: out(7-0)
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity decoder_1 is
   port (
         i_in:    in std_logic_vector(2 downto 0);
         o_out:   out std_logic_vector(7 downto 0)
         );
end entity;
```

VHDL Decoders

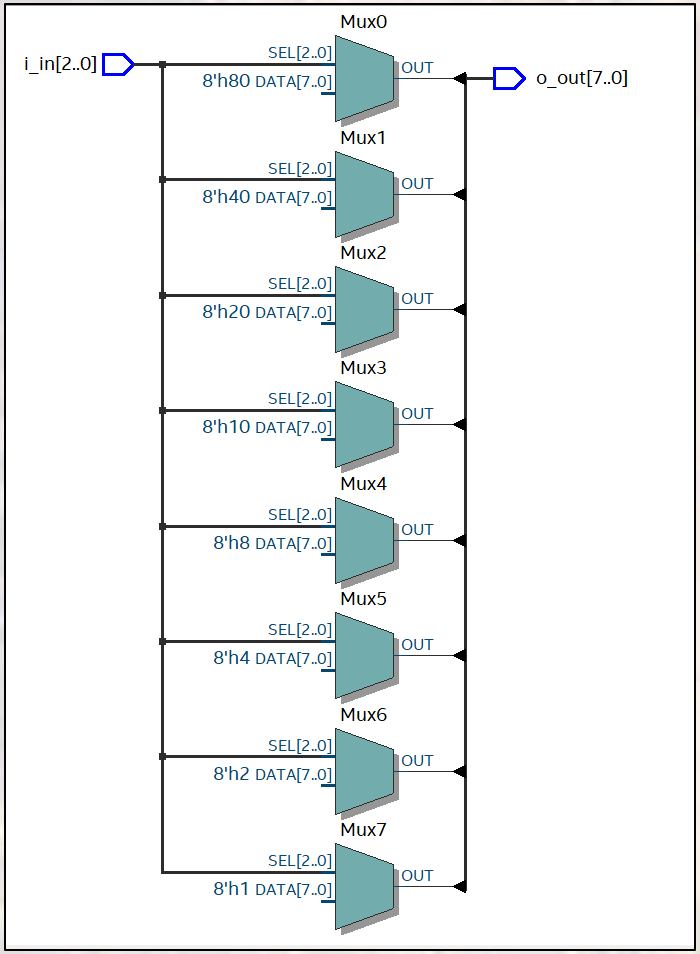
- 3-8 Example
  - Architecture

```
architecture behavioral of decoder_1 is

begin

    with i_in select o_out <=
                          "00000001" when "000",
                          "00000010" when "001",
                          "00000100" when "010",
                          "00001000" when "011",
                          "00010000" when "100",
                          "00100000" when "101",
                          "01000000" when "110",
                          "10000000" when "111",
                          "00000000" when others;

end behavioral;
```

exhaustive list

VHDL Decoders

- 3-8 Example



Flow Summary

<<Filter>>

Flow Status	Successful - Thu Jan 02 11:48:21 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	decoder_1
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	8
Total registers	0
Total pins	11
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0