VHDL Development Process - Logic

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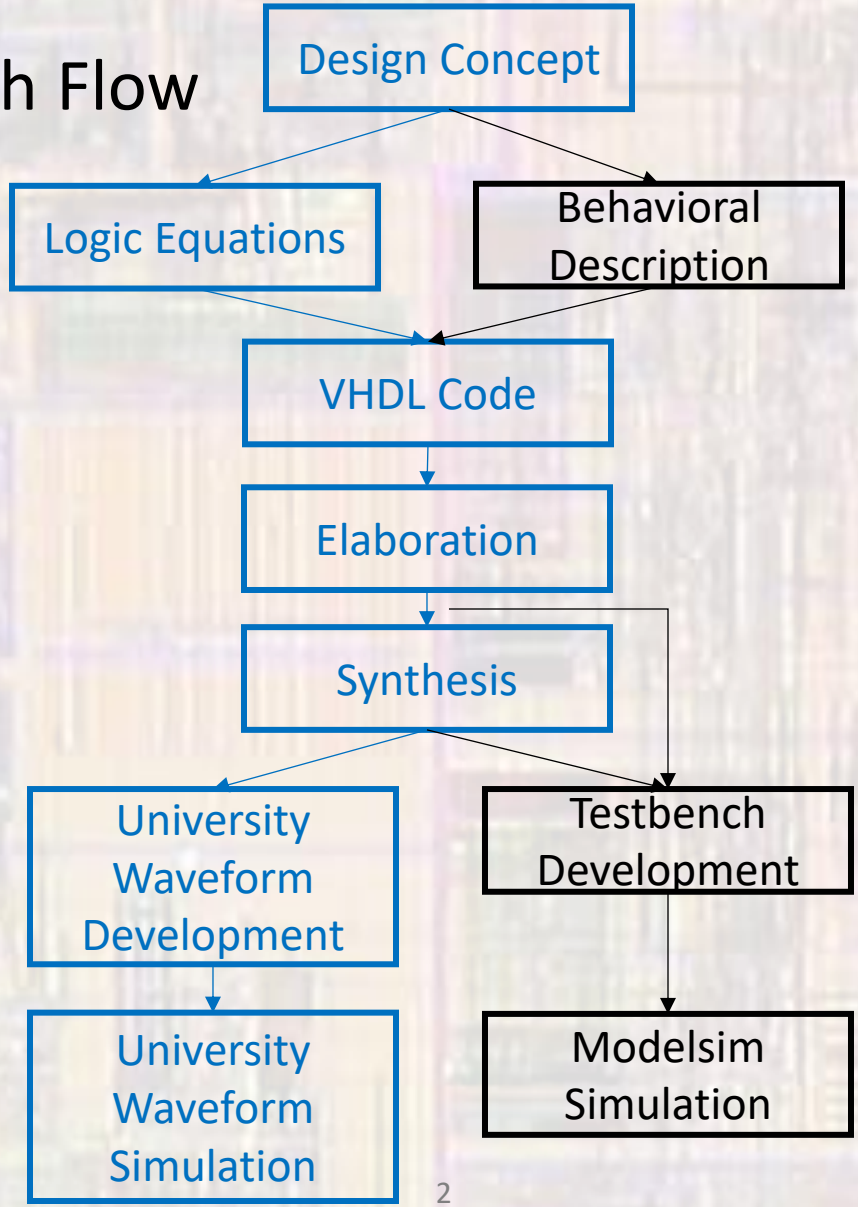
- Multi-path Flow



VHDL Development Process - Logic

- Quartus Tools
  - Analysis
    - Checks for syntax errors
  - Elaboration
    - Creates a mathematical model of the VHDL description
    - Used for functional simulation and verification
  - Synthesis
    - Creates a gate level implementation
      - Multiplexor based for FPGAs
      - Not tied to any specific circuits on the FPGA
  - Testbench
    - VHDL code for creating and evaluating simulations
  - Modelsim
    - Full function simulation tool
  - University Waveform Viewer
    - Simplified simulation interface for Modelsim