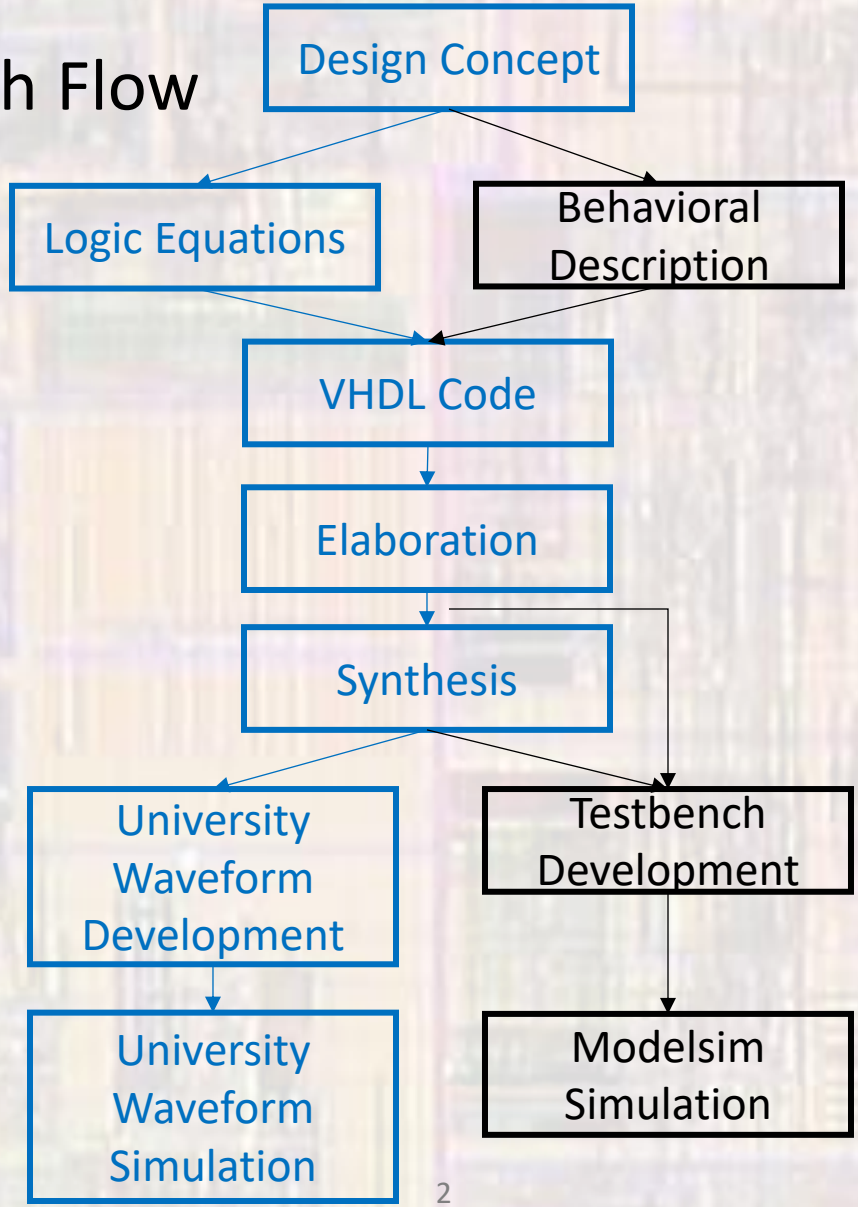
VHDL Development Process – Logic Examples

Last updated 12/31/24

VHDL Development Process – Logic - Examples

- Multi-path Flow



VHDL Development Process – Logic - Examples

- Odd/Even Detector
  - Outputs a 1 if the number of 1's input is even
  - Design Equations

$$oddeven\_out = \overline{odd}$$

$$odd = ab \otimes cd$$

$$ab = a \otimes b$$

$$cd = c \otimes d$$

VHDL Development Process – Logic - Examples

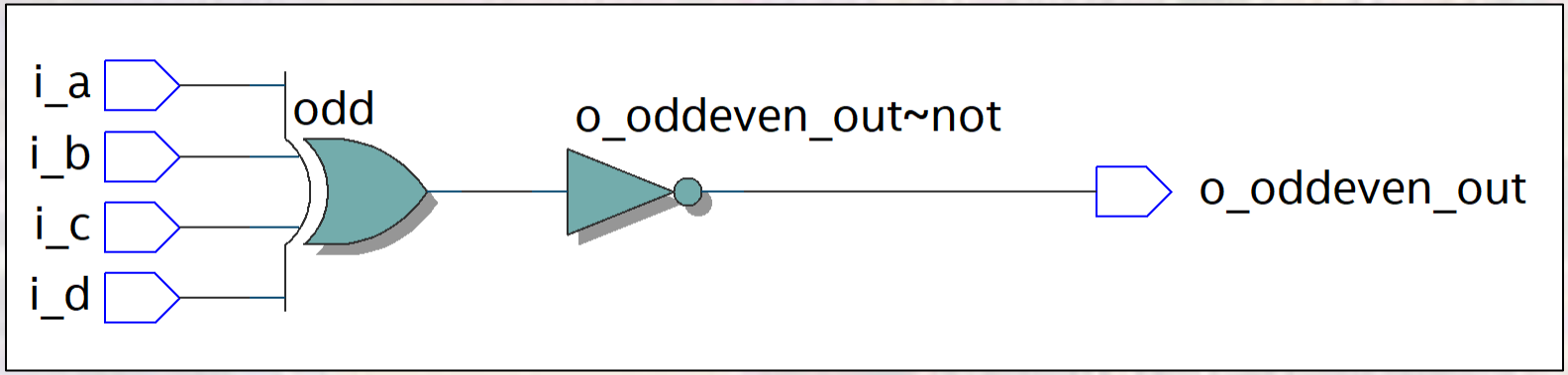
- Odd/Even Detector

```
--
--  oddeven_4bit_logic.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  4 bit odd even detector
--  outputs 1 if # of 1's is even
--
--  inputs: a, b, c, d
--
--  outputs: oddeven_out
--
----------------------------------
library IEEE;
use ieee.std_logic_1164.all;

entity oddeven_4bit_logic is
   port( i_a:          in std_logic;
         i_b:          in std_logic;
         i_c:          in std_logic;
         i_d:          in std_logic;
         o_oddeven_out: out std_logic
   );
end entity;
```

```
architecture logic of oddeven_4bit_logic is

   -- internal signals
   signal ab:  std_logic;
   signal cd:  std_logic;
   signal odd: std_logic;

begin

   o_oddeven_out <= NOT odd;
   odd <= ab XOR cd;

   ab <= i_a XOR i_b;
   cd <= i_c XOR i_d;

end architecture;
```

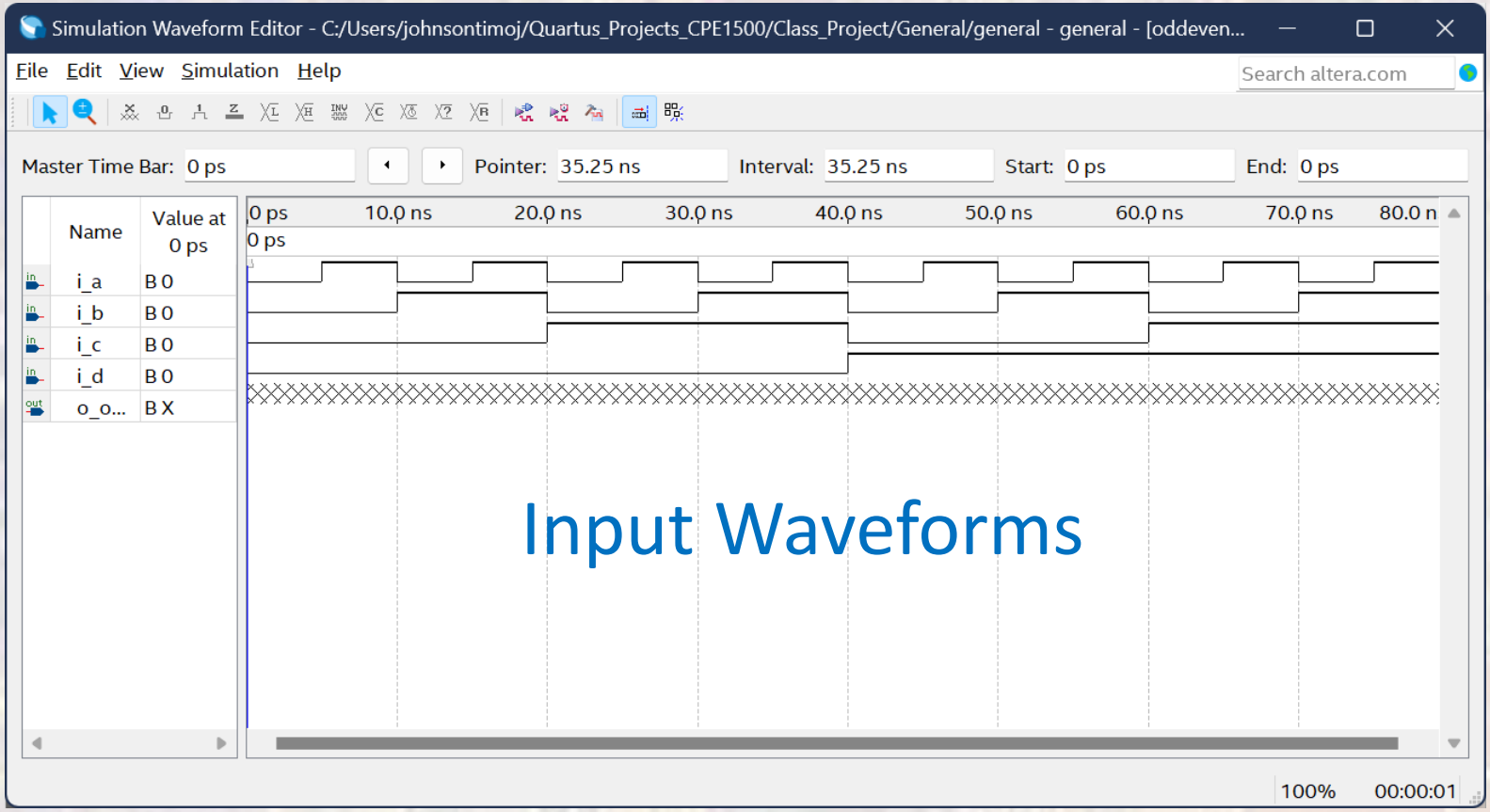
VHDL Development Process – Logic - Examples

- Odd/Even Detector



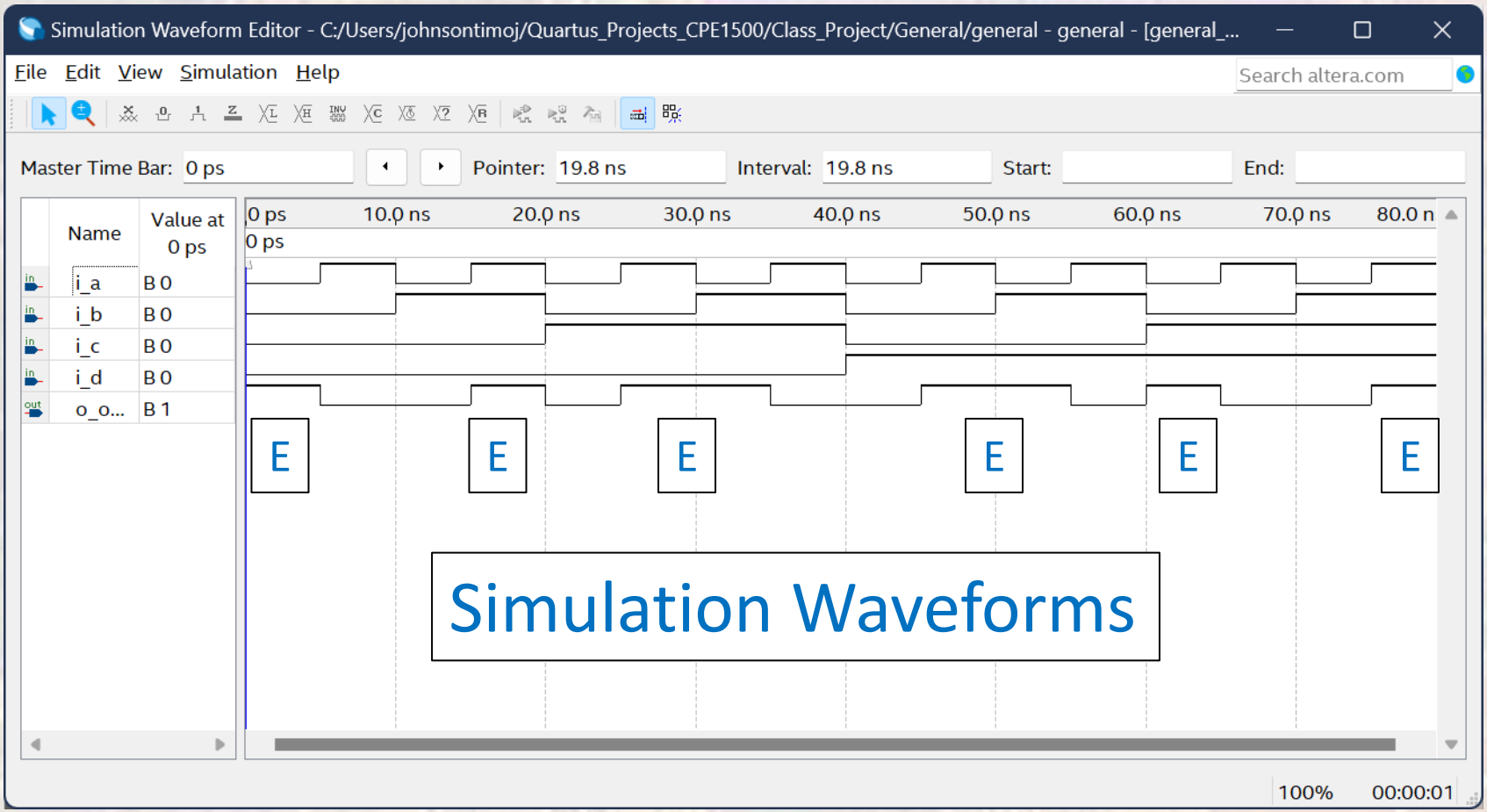
VHDL Development Process – Logic - Examples

- Odd/Even Detector



VHDL Development Process – Logic - Examples

- Odd/Even Detector



VHDL Development Process – Logic - Examples

- Multiplexor
  - Design Equations

out = selA + selB + selC + selD

selA = A $\overline{sel(1)}$ $\overline{sel(0)}$

selB = B $\overline{sel(1)}$ sel(0)

selC = C sel(1) $\overline{sel(0)}$

selD = D sel(1) sel(0)

VHDL Development Process – Logic - Examples

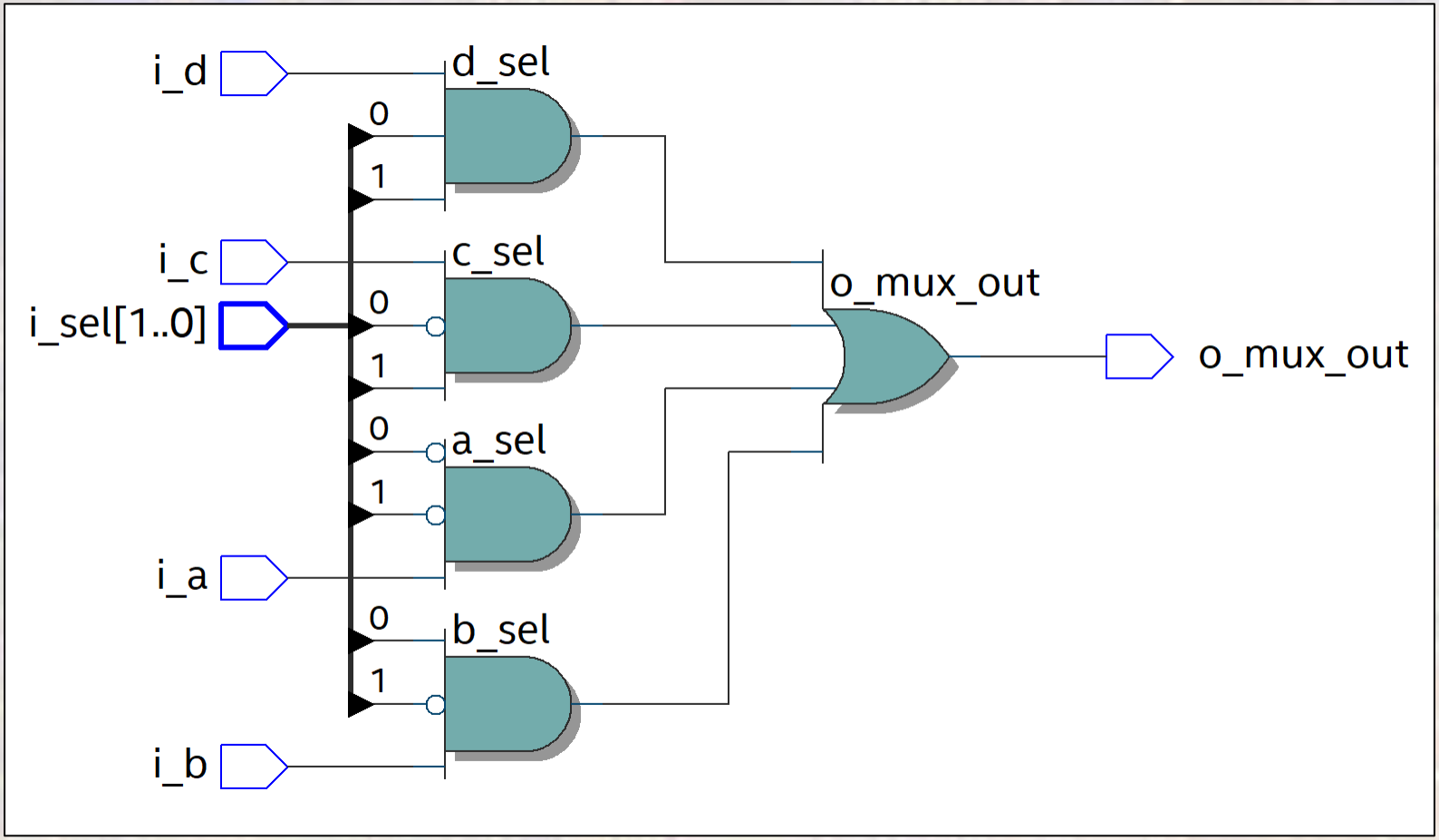
- Multiplexor

```
--------------------------------
--
--  multiplexor_4bit_logic.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
--------------------------------
--
--  4 bit multiplexor
--
--  inputs: a, b, c, d, sel1, sel0
--
--  outputs: mux_out
--
--------------------------------
library IEEE;
use ieee.std_logic_1164.all;

entity multiplexor_4bit_logic is
   port( i_a:        in std_logic;
         i_b:        in std_logic;
         i_c:        in std_logic;
         i_d:        in std_logic;
         i_sel:      in std_logic_vector(1 downto 0);
         o_mux_out:  out std_logic
   );
end entity;
```

```
architecture logic of multiplexor_4bit_logic is

   -- internal signals
   signal sel0_b: std_logic;
   signal sel1_b: std_logic;
   signal a_sel:  std_logic;
   signal b_sel:  std_logic;
   signal c_sel:  std_logic;
   signal d_sel:  std_logic;

begin

   sel0_b <= not i_sel(0);
   sel1_b <= not i_sel(1);

   o_mux_out <= a_sel OR b_sel OR c_sel OR d_sel;

   a_sel <= i_a AND sel1_b AND sel0_b;
   b_sel <= i_b AND sel1_b AND i_sel(0);
   c_sel <= i_c AND i_sel(1) AND sel0_b;
   d_sel <= i_d AND i_sel(1) AND i_sel(0);

end architecture;
```

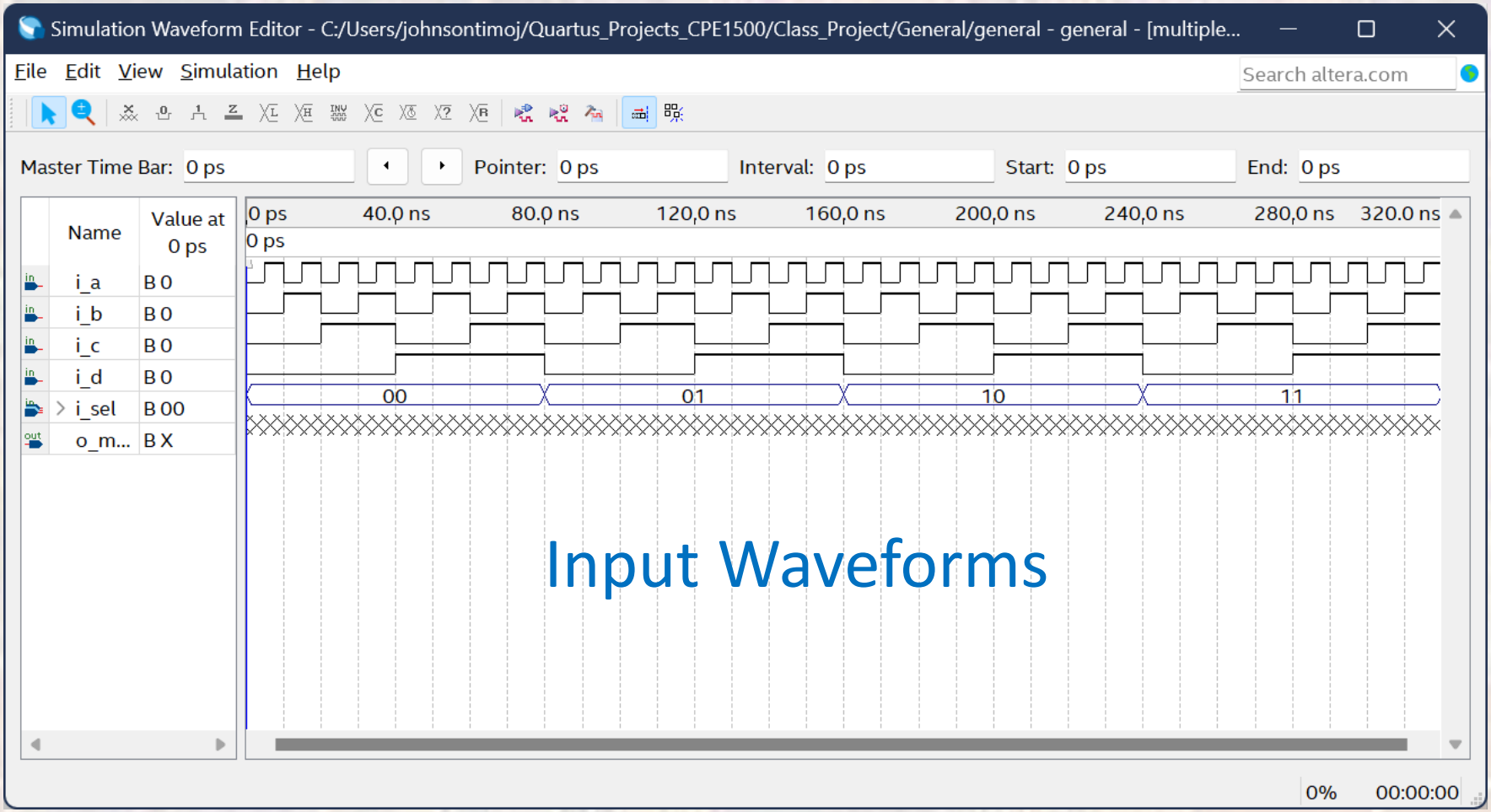
VHDL Development Process – Logic - Examples

- Multiplexor



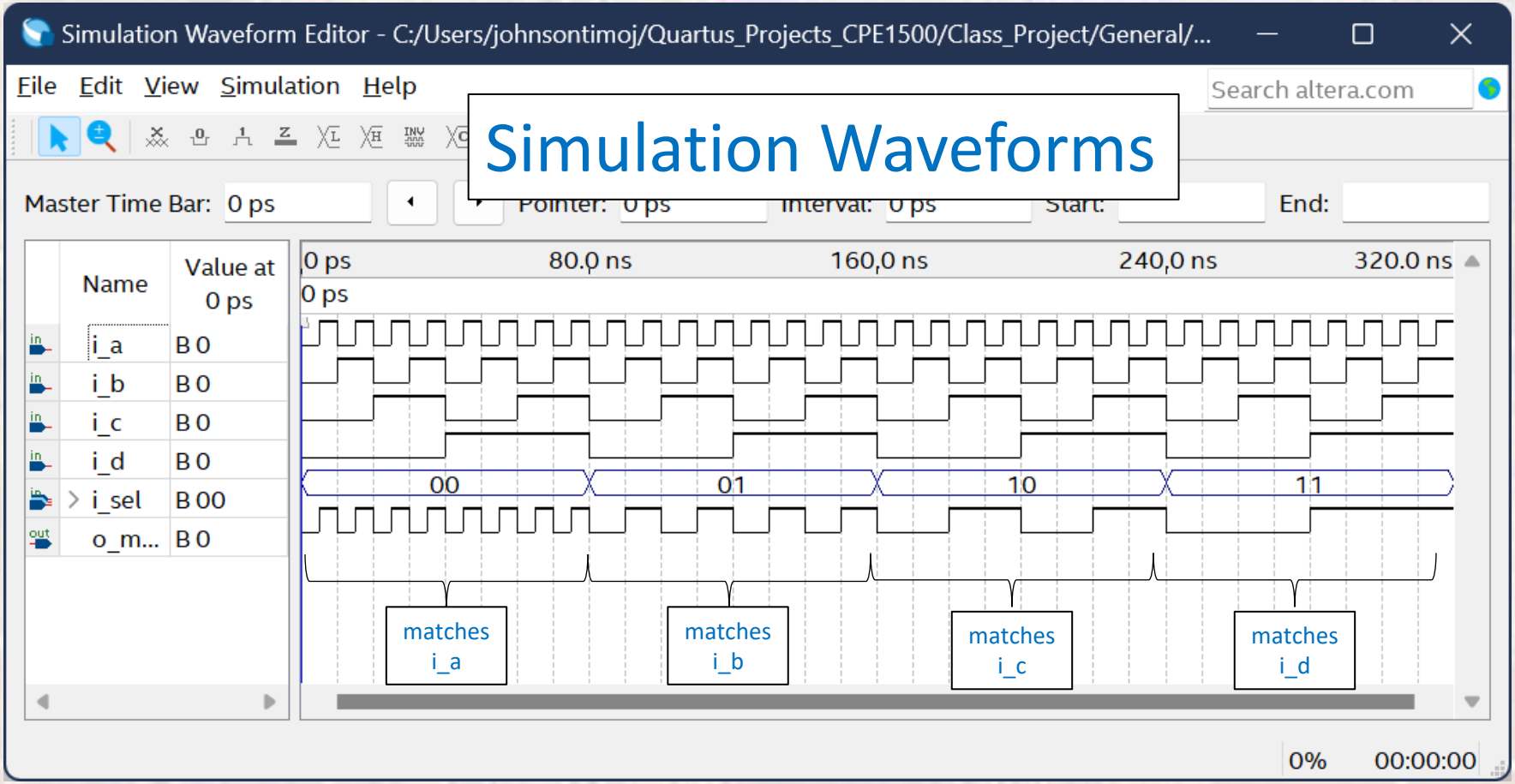
VHDL Development Process – Logic - Examples

- Multiplexor



VHDL Development Process – Logic - Examples

- Multiplexor



VHDL Development Process – Logic - Examples

- Odd/Even Detector – 16 bit structural
  - Outputs a 1 if the number of 1's input is even
  - Design Equations

  4 oddeven detectors feeding a 5^{th} oddeven detector

VHDL Development Process – Logic - Examples

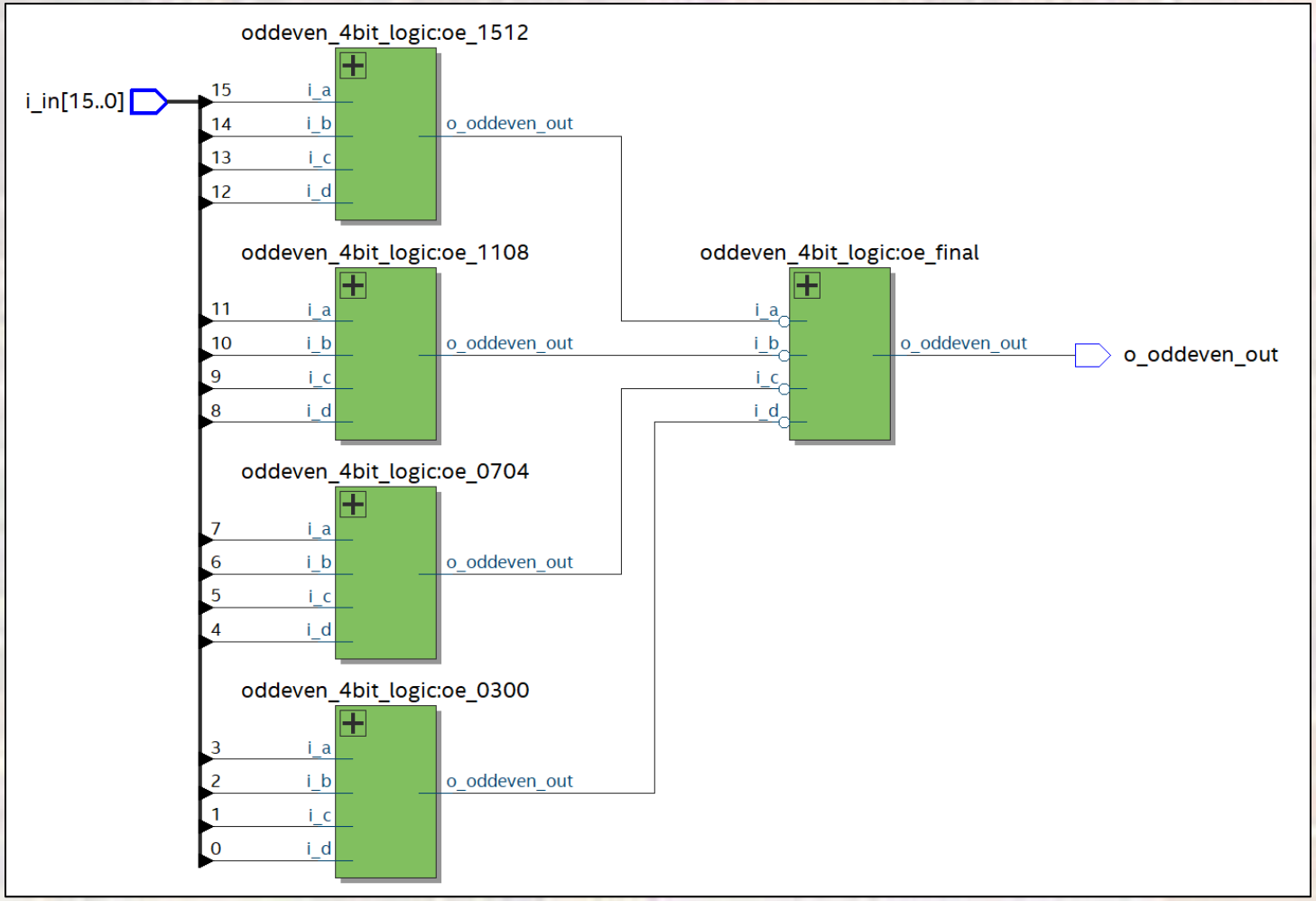
- Odd/Even Detector – 16 bit structural

```
----------------------------------
--
--  oddeven_4bit_logic_structural.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  16 bit odd even detector using structural VHDL
--  outputs 1 if # of 1's is even
--
--  inputs: in(0) -> in(15)
--
--  outputs: oddeven_out
--
----------------------------------
library IEEE;
use ieee.std_logic_1164.all;

entity oddeven_16bit_logic_structural is
   port( i_in:          in std_logic_vector(15 downto 0);
         o_oddeven_out: out std_logic
   );
end entity;

architecture logic of oddeven_16bit_logic_structural is

   -- internal signals
   signal sig_15_12: std_logic;
   signal sig_11_8:  std_logic;
   signal sig_7_4:   std_logic;
   signal sig_3_0:   std_logic;

   component oddeven_4bit_logic is
   port( i_a:           in std_logic;
         i_b:           in std_logic;
         i_c:           in std_logic;
         i_d:           in std_logic;
         o_oddeven_out: out std_logic
      );
   end component;
```

```
begin

   oe_1512: oddeven_4bit_logic
   port map(   i_a           => i_in(15),
               i_b           => i_in(14),
               i_c           => i_in(13),
               i_d           => i_in(12),
               o_oddeven_out => sig_15_12
           );

   oe_1108: oddeven_4bit_logic
   port map(   i_a           => i_in(11),
               i_b           => i_in(10),
               i_c           => i_in(9),
               i_d           => i_in(8),
               o_oddeven_out => sig_11_8
           );

   oe_0704: oddeven_4bit_logic
   port map(   i_a           => i_in(7),
               i_b           => i_in(6),
               i_c           => i_in(5),
               i_d           => i_in(4),
               o_oddeven_out => sig_7_4
           );

   oe_0300: oddeven_4bit_logic
   port map(   i_a           => i_in(3),
               i_b           => i_in(2),
               i_c           => i_in(1),
               i_d           => i_in(0),
               o_oddeven_out => sig_3_0
           );

   oe_final: oddeven_4bit_logic
   port map(   i_a           => NOT sig_15_12,
               i_b           => NOT sig_11_8,
               i_c           => NOT sig_7_4,
               i_d           => NOT sig_3_0,
               o_oddeven_out => o_oddeven_out
           );

end architecture;
```

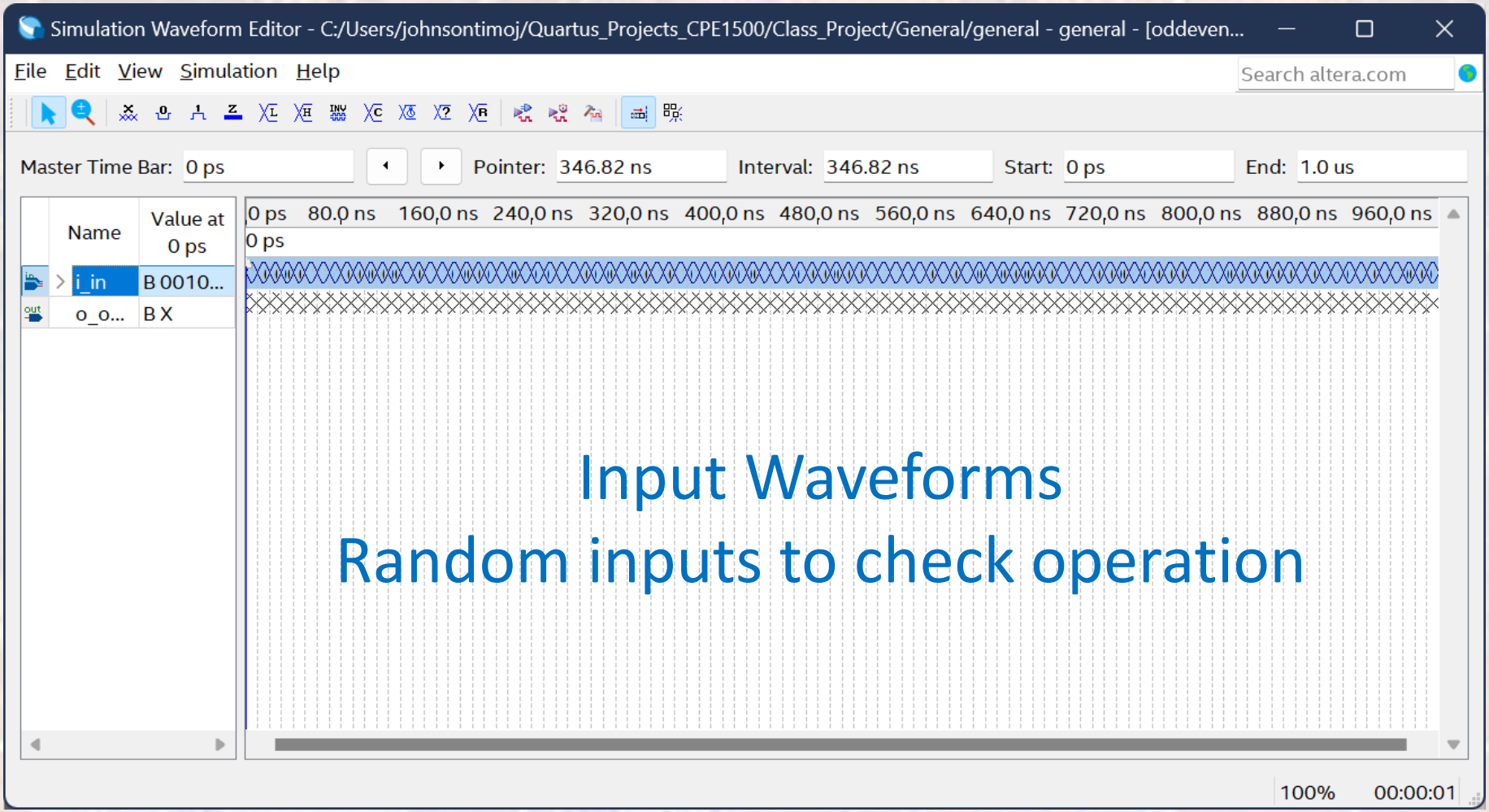
VHDL Development Process – Logic - Examples

- Odd/Even Detector – 16 bit structural



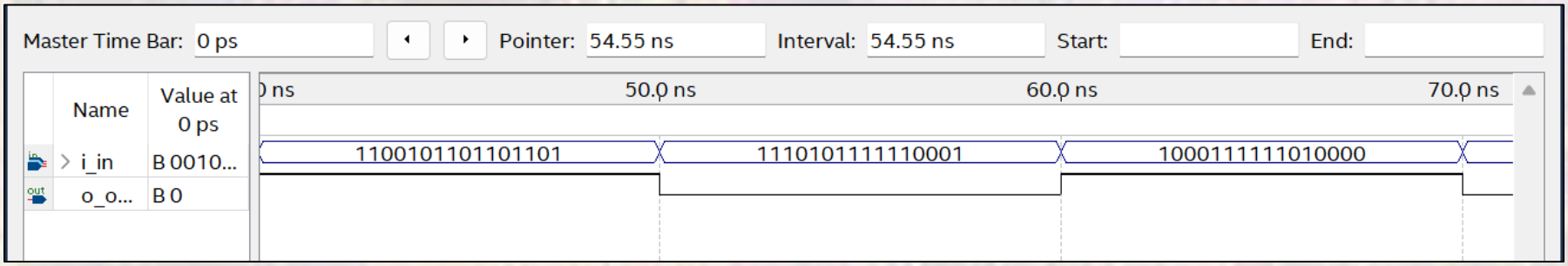
VHDL Development Process – Logic - Examples

- Odd/Even Detector – 16 bit structural



VHDL Development Process – Logic - Examples

- Odd/Even Detector – 16 bit structural



Simulation Waveforms