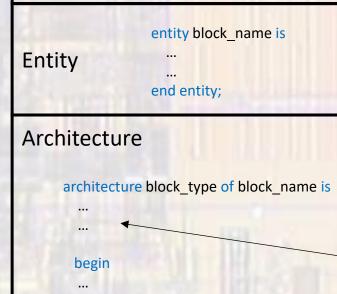
VHDL File Structure



Description and comments

Library Inclusions

end entity;



block_name must match the file name

Describes the external view of the block Input/Output Ports

Parameters (Generics)

Describes the operation of the block

block_type is user defined Used to describe the kind of VHDL being described Typical values: behavioral, structural, testbench

Declare constants and signals Declare any included structural blocks

Describe the desired hardware actions Describe the interconnect between structural blocks