VHDL Logic Operators

- VHDL supports 7 logic operators

NOT

AND NAND

OR NOR

XOR XNOR

- There is no precedence or associativity defined for the logical operators
  - Parenthesis are required when combining more than one operator type in a statement

OK

```
o_mux_out <= a_sel OR b_sel OR c_sel OR d_sel;
```

Error

```
o_mux_out <= a_sel OR b_sel AND c_sel XOR d_sel;
```

OK

```
o_mux_out <= ((a_sel OR b_sel) AND c_sel) XOR d_sel;
```

VHDL Logic Operators

- The Logic Operators can operate on individual wires (std_logic)

```
signal in1:    std_logic;
signal in2:    std_logic;
signal out1:   std_logic;
```

```
out1 <= in1 AND in2;
```

- The Logical Operators can operate on groups of wires or buses (std_logic_vector)
  - The operation is performed bit-by-bit (bitwise)

```
signal inA:      std_logic_vector(7 downto 0);
signal inB:      std_logic_vector(7 downto 0);
signal out_AB:   std_logic_vector(7 downto 0);
```

```
out_AB <= inA OR inB;
```