VHDL Numeric Types

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VHDL Numeric Types

- Standard Logic Vector
  - Represents a group of wires
  - Has no numeric interpretation
  - Cannot be added or subtracted
  - Cannot be compared reliably
- A new library
  - ieee.numeric_std.all
  - 2 new vector types
    - unsigned
    - signed
  - Represent unsigned and signed binary numbers

VHDL Numeric Types

- Numeric_Std Types
  - unsigned array of std_logic (analogous to a std_logic_vector)
  - signed array of std_logic (analogous to a std_logic_vector)

- Values
  - unsigned is interpreted as unsigned magnitude (always positive)
  - signed is interpreted as 2's complement (positive and negative)

VHDL Numeric Types

- Operators
  - Boolean: not†, and, or, nand, nor, xor, xnor
  - Comparison: =, /=, <, <=, >, >=
  - Concatenation: &
  - Shift left, shift right logical: sll, srl
  - Rotate left, rotate right: rol, ror
  - Arithmetic †† : +, -, mod, rem,
    : *†††, /†††
    : **††††
    : sign -†††††, abs†††††

† negation of 2's complement most negative value will return the most negative value

†† Arithmetic operators other than multiplication preserve the length of the result vector i.e. wrap

††† * and / will create large logical solutions

†††† only use with a base of 2

††††† signed only

VHDL Numeric Types

- Functions
  - shift_left shift left
  - shift_right shift right arithmetic
  - rotate_left rotate left
  - rotate_right rotate right

  - resize resize unsigned using zero extension
    resize signed using sign extension