VHDL - Others

- Others is a catch-all term in VHDL
  - It is used to indicate all possible values that are not otherwise enumerated

Set all bits of a vector to ‘0’

```
my_6bit_slv <= (others => '0');
```

Used to specify all other possible values

```
with i_inC select o_outV <=
   "0001" when "0000",
   "0010" when "0001",
   "1001" when "1000",
   "0000" when others;
```