VHDL Shift Registers

Last updated 1/9/25

VHDL Shift Registers

- Shift Register
  - Shift a series of bits within a register
  - Left/right
  - N bit shift
  - Wrapping (rotate)
    - Load register with load signal
    - Direction
  - Non-wrapping
    - Data input – both sides
    - Direction

DATA	dir	load	Din	result
XXXXX	X	1	00100	00101
00101	R	0	XXXXX	10010
00101	L	0	XXXXX	01010

Din	DATA	dir	result
1	00100	R	10010
0	10010	R	01001
1	01001	L	10011

VHDL Shift Registers

- Non-wrapping - 4 bit
- D shifts in from left or right

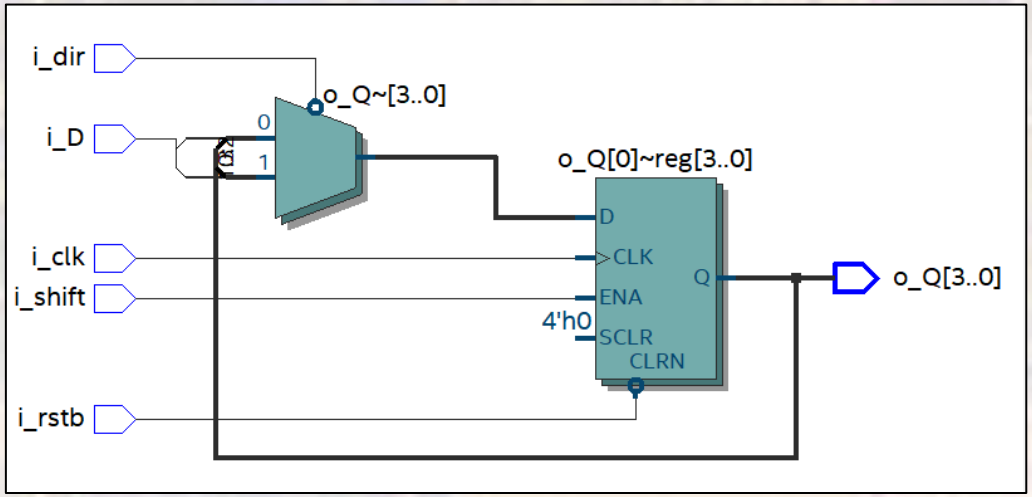
```
----------------------------------
--
--  reg_shift_4bit.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  standard 4 bit shift register
--  inputs: clk, rstb, shift, dir, d
--          dir: 0 -> L, 1 -> R
--
--  outputs: q
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity reg_shift_4bit is
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;
      i_shift: in std_logic;
      i_dir:   in std_logic;   -- 0 -> L
      i_D :    in std_logic;

      o_Q :    out std_logic_vector(3 downto 0)
   );
end entity;

architecture behavioral of reg_shift_4bit is
```

using brute force concatenation to perform the shift

```
architecture behavioral of reg_shift_4bit is

begin

   process (i_clk, i_rstb)
   begin
      -- asynch
      if (i_rstb = '0') then
         o_Q <= "0000";
      -- synch
      elsif (rising_edge(i_clk)) then
         -- shift?
         if(i_shift = '1') then
            -- L
            if(i_dir = '0') then
               o_Q <= o_Q(2) & o_Q(1) & o_Q(0) & i_D;
            else
               o_Q <= i_D & o_Q(3) & o_Q(2) & o_Q(1);
            end if;   -- dir
         end if;      -- shift - no else needed - FF template being used
      end if;         -- main - no else needed - FF template being used
   end process;

end architecture;
```

VHDL Shift Registers

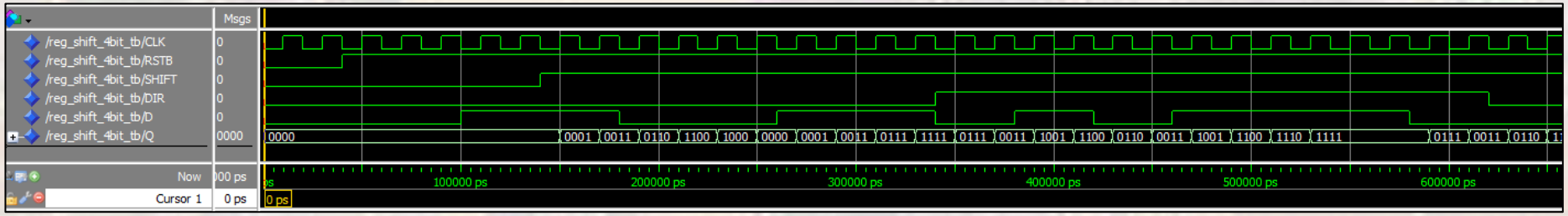
- 4 bit
- D shifts in from left or right



Flow Summary

<<Filter>>

Flow Status	Successful - Thu Jan 09 12:33:06 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	reg_shift_4bit
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	4
Total registers	4
Total pins	9
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



no shift

left shift

right shift

VHDL Shift Registers

- n bit
  - D shifts in from left or right

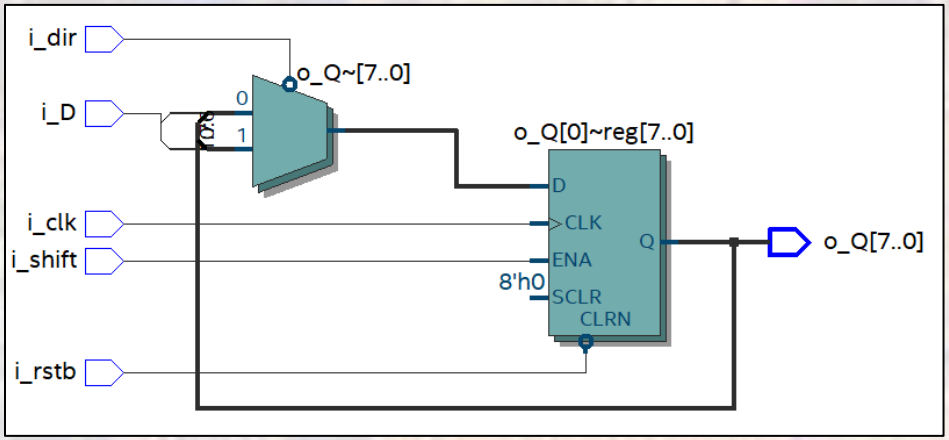
using concatenation to perform the shift

```
----------------------------------
--
--  reg_shift_nbit.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  standard N bit shift register
--  inputs: clk, rstb, shift, dir, d
--          dir: 0 -> L, 1 -> R
--
--  outputs: q
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity reg_shift_nbit is
   generic(
            N: positive := 8
          );
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;
      i_shift: in std_logic;
      i_dir:   in std_logic;   -- 0 -> L
      i_D :    in std_logic;

      o_Q :    out std_logic_vector((N - 1) downto 0)
   );
end entity;
```

```
architecture behavioral of reg_shift_nbit is

begin

   process (i_clk, i_rstb)
   begin
      -- asynch
      if (i_rstb = '0') then
         o_Q <= (others => '0');
      -- synch
      elsif (rising_edge(i_clk)) then
         -- shift?
         if(i_shift = '1') then
            -- L
            if(i_dir = '0') then
               o_Q <= o_Q(((N - 1) - 1) downto 0) & i_D;
            else
               o_Q <= i_D & o_Q((N - 1) downto 1);
            end if;   -- dir
         end if;      -- shift - no else needed - FF template being used
      end if;         -- main - no else needed - FF template being used
   end process;

end architecture;
```

VHDL Shift Registers

- n – bit (N = 8)
  - D shifts in from left or right



Flow Summary

<<Filter>>

Flow Status	Successful - Thu Jan 09 12:51:15 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	reg_shift_nbit
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	8
Total registers	8
Total pins	13
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

VHDL Shift Registers

- n- bit w/load

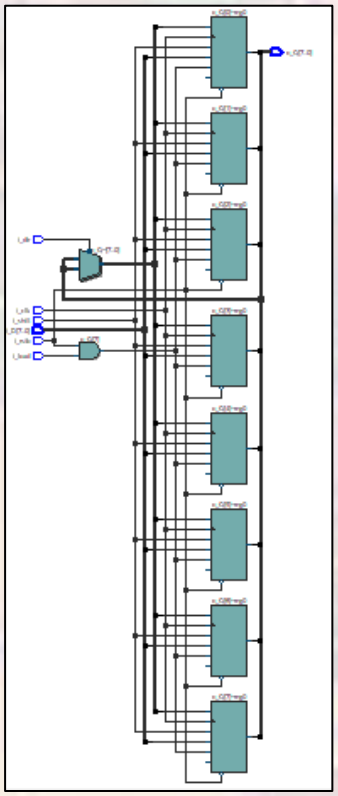
```
----------------------------------
--
--  reg_shift_nbit_load.vhdl
--
--  by: johnsontimoj
--
--  created: 12/31/24
--
--  version: 0.0
--
----------------------------------
--
--  standard N bit shift register with load
--  inputs: clk, rstb, shift, dir, d
--          dir: 0 -> L, 1 -> R
--
--  outputs: q
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity reg_shift_nbit_load is
   generic(
            N: positive := 8
          );
   port(
      i_clk:   in std_logic;
      i_rstb:  in std_logic;
      i_shift: in std_logic;
      i_dir:   in std_logic;   -- 0 -> L
      i_load:  in std_logic;
      i_D :    in std_logic_vector((N - 1) downto 0);

      o_Q :    out std_logic_vector((N - 1) downto 0)
   );
end entity;
```

asynchronous load

```
architecture behavioral of reg_shift_nbit_load is

begin

   process (i_clk, i_rstb, i_load)
   begin
      -- asynch
      if (i_rstb = '0') then
         o_Q <= (others => '0');
      elsif(i_load = '1') then
         o_Q <= i_D;
      -- synch
      elsif (rising_edge(i_clk)) then
         -- shift?
         if(i_shift = '1') then
            -- L
            if(i_dir = '0') then
               o_Q <= o_Q(((N - 1) - 1) downto 0) & o_Q(N - 1);
            else
               o_Q <= o_Q(0) & o_Q((N - 1) downto 1);
            end if;   -- dir
         end if;      -- shift - no else needed - FF template being used
      end if;         -- main - no else needed - FF template being used
   end process;

end architecture;
```

VHDL Shift Registers

- n- bit w/load



Flow Summary

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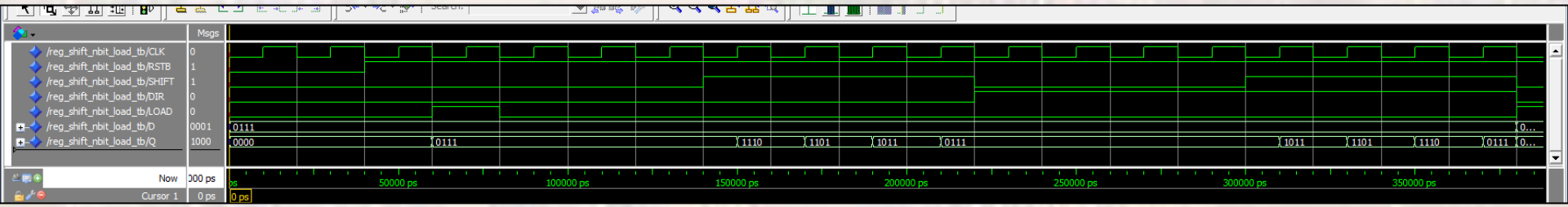
Flow Status	Successful - Thu Jan 09 13:03:24 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	reg_shift_nbit_load
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	34
Total registers	8
Total pins	21
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

reset

load



no shift

left shift

no shift

right shift