VHDL Shifters

Last updated 1/7/25

VHDL Shifters

- Logical Shift L/R
- Arithmetic Shift L/R
- Rotate L/R

VHDL Shifters

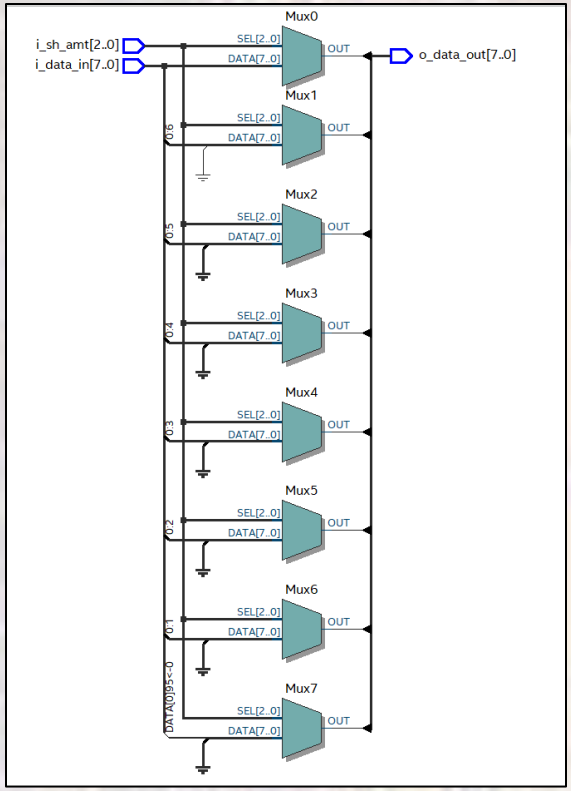
- Logical Shift Left

```
--------------------------------------
--
-- shift_left_logical.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
--------------------------------------
--
-- vhdl logical shift left - brute-force
--
--------------------------------------
--
-- Inputs:  in(7-0)
--          shift amount (2-0)
-- Outputs: out(7-0)
--
--------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity shift_left_logical is
   port (
         i_data_in:     in std_logic_vector(7 downto 0);
         i_sh_amt:      in std_logic_vector(2 downto 0);
         o_data_out:    out std_logic_vector(7 downto 0)
         );
end entity;
```

```
architecture behavioral of shift_left_logical is

begin

   with i_sh_amt select o_data_out <=
            i_data_in(7 downto 0)              when "000",
            i_data_in(6 downto 0) & "0"        when "001",
            i_data_in(5 downto 0) & "00"       when "010",
            i_data_in(4 downto 0) & "000"      when "011",
            i_data_in(3 downto 0) & "0000"     when "100",
            i_data_in(2 downto 0) & "00000"    when "101",
            i_data_in(1 downto 0) & "000000"   when "110",
            i_data_in(0 downto 0) & "0000000"  when "111",
            i_data_in(7 downto 0)              when others;

end behavioral;
```

VHDL Shifters

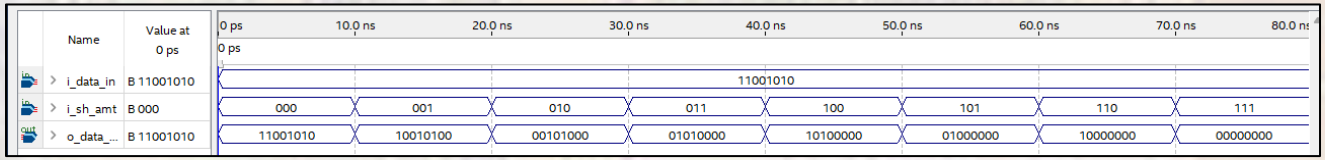
- Logical Shift Left



Flow Summary

<<Filter>>

Flow Status	Successful - Fri Jan 03 09:16:21 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	shift_left_logical
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	21
Total registers	0
Total pins	19
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



VHDL Shifters

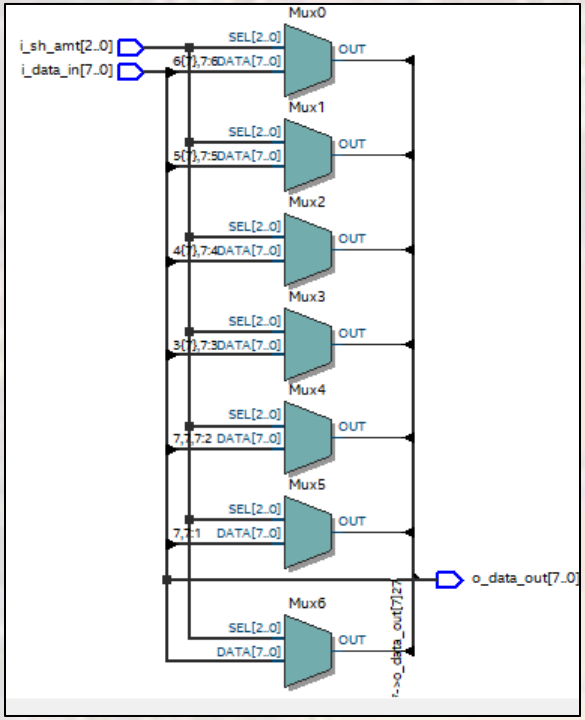
- Arithmetic Shift Right

```
----------------------------------------
--
-- shift_right_arithmetic.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
----------------------------------------
--
-- vhdl arithmetic shift right - brute-force
--
----------------------------------------
--
-- Inputs:  in(7-0)
--          shift amount (2-0)
-- Outputs: out(7-0)
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity shift_right_arithmetic is
   port (
         i_data_in:     in std_logic_vector(7 downto 0);
         i_sh_amt:      in std_logic_vector(2 downto 0);
         o_data_out:    out std_logic_vector(7 downto 0)
         );
end entity;
```

```
architecture behavioral of shift_right_arithmetic is

begin

   with i_sh_amt select o_data_out <=
            i_data_in(7 downto 0)   when "000",
            i_data_in(7) & i_data_in(7 downto 1) when "001",
            i_data_in(7) & i_data_in(7) & i_data_in(7 downto 2) when "010",
            i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7 downto 3) when "011",
            i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7 downto 4) when "100",
            i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7 downto 5) when "101",
            i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7 downto 6) when "110",
            i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7) & i_data_in(7 downto 7) when "111",
            i_data_in(7 downto 0)   when others;

end behavioral;
```

VHDL Shifters

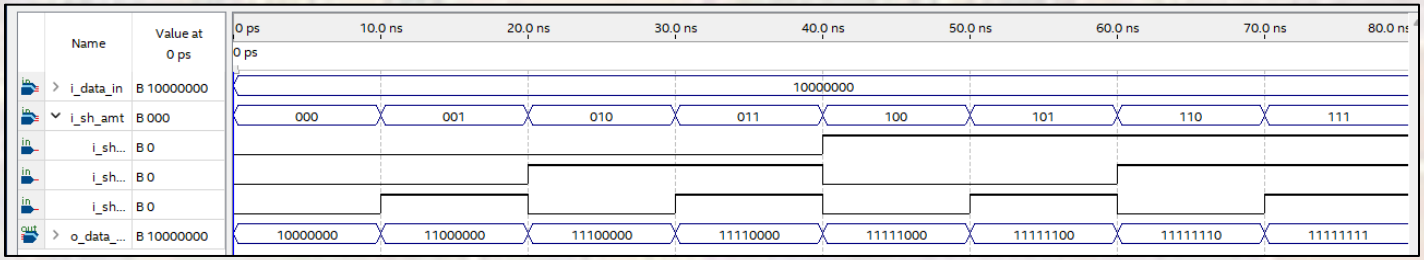
- Arithmetic Shift Right



Flow Summary

<<Filter>>

Flow Status	Successful - Tue Jan 07 13:08:18 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	shift_right_arithmetic
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	20
Total registers	0
Total pins	19
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



VHDL Shifters

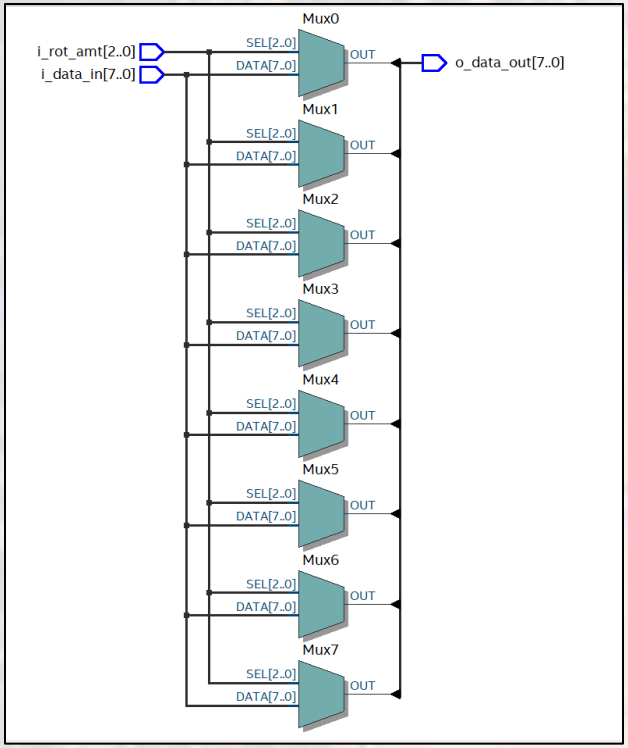
- Rotate Left

```
----------------------------------------
--
-- rotator_left.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
----------------------------------------
--
-- vhdl rotator - left - brute-force
--
----------------------------------------
--
-- Inputs:  in(7-0)
--          rotate amount (2-0)
-- Outputs: out(7-0)
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity rotator_left is
   port (
         i_data_in:     in std_logic_vector(7 downto 0);
         i_rot_amt:     in std_logic_vector(2 downto 0);
         o_data_out:    out std_logic_vector(7 downto 0)
         );
end entity;
```

```
architecture behavioral of rotator_left is

begin

   with i_rot_amt select o_data_out <=
            i_data_in(7 downto 0)                                  when "000",
            i_data_in(6 downto 0) & i_data_in(7 downto 7)   when "001",
            i_data_in(5 downto 0) & i_data_in(7 downto 6)   when "010",
            i_data_in(4 downto 0) & i_data_in(7 downto 5)   when "011",
            i_data_in(3 downto 0) & i_data_in(7 downto 4)   when "100",
            i_data_in(2 downto 0) & i_data_in(7 downto 3)   when "101",
            i_data_in(1 downto 0) & i_data_in(7 downto 2)   when "110",
            i_data_in(0 downto 0) & i_data_in(7 downto 1)   when "111",
            i_data_in(7 downto 0)                                  when others;

end behavioral;
```

VHDL Shifters

- Rotate Left



Flow Summary

<<Filter>>

Flow Status	Successful - Fri Jan 03 09:42:15 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	general
Top-level Entity Name	rotator_left
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	24
Total registers	0
Total pins	19
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0