VHDL Vector Manipulation

- Bit access

  my_slv(4) selects bit 4 from vector my_slv

  selects a single wire

- Vector access

  my_slv(3 downto 1) selects bits 3, 2, 1 of vector my_slv

  selects a group of wires

  my_slv(4 downto 4) selects a single wire

- Vector extension (concatenation)
  - &

```
my_4bit_slv <= a & b & c & d;
my_8bit_slv <= e & f & my_4bit_slv & g & h;
my_6bit_slv <= e & f & my_4bit_slv(2 downto 1) & g & h;
my_7bit_slv(3 downto 0) <= my_4bit_slv;
```