VHDL Selection – when-else

- when-else
  - Choose a value when a certain situation exists

```
result_signal   <=   result_value when decision_signal = decision_value else
                     result_value when decision_signal = decision_value else
                     result_value when decision_signal = decision_value else
                     result_value;
```

Limitation: Only one result signal

VHDL Selection – when-else

- when-else

Exhaustive List

```
outA <= "1000" when inA = "00" else
        "0100" when inA = "01" else
        "0010" when inA = "10" else
        "0010" when inA = "11" else
        "0001";
```

Partial List

```
outA <= "1000" when inA = "00" else
        "0100" when inA = "01" else
        "0001";
```

Partially Common Result

```
outA <= "1000" when inA = "00" else
        "0100" when inA = "01" else
        "0010" when inA = ("10"  or "11") else
        "0001";
```

Complex Selection

```
outA <= "1000" when (inA or inB) = "00" else
        "0100" when (inA or inB) = "01" else
        "0010" when (inA or inB) = "10" else
        "0001";
```

VHDL Selection – when-else

- when-else

Exhaustive List

```
outA <= sig1 when inA = "00" else
        sig2 when inA = "01" else
        sig3 when inA = "10" else
        sig4 when inA = "11" else
        sigx;
```

Partial List

```
outA <= sig1 when inA = "00" else
        sig2 when inA = "01" else
        sigx;
```

Partially Common Result

```
outA <= sig1 when inA = "00" else
        sig2 when inA = "01" else
        sig3 when inA = ("10"  or "11") else
        sigx;
```

Complex Selection

```
outA <= sig1 when (inA or inB) = "00" else
        sig2 when (inA or inB) = "01" else
        sig3 when (inA or inB) = "10" else
        sigx;
```

VHDL Selection – when-else

- when-else - example

```
----------------------------------------
--
-- with_select_example.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
----------------------------------------
--
-- with-select example
--
----------------------------------------
--
-- Inputs: inC
-- Outputs: outV
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity with_select_example is
   port (
         i_inC:   in std_logic_vector(3 downto 0);
         o_outV: out std_logic_vector(3 downto 0)
   );
end entity;
```

```
architecture behavioral of with_select_example is

begin
   with i_inC select o_outV <=
      "0001" when "0000",
      "0010" when "0001",
      "0011" when "0010",
      "0100" when "0011",
      "0101" when "0100",
      "0110" when "0101",
      "0111" when "0110",
      "1000" when "0111",
      "1001" when "1000",
      "0000" when others;

end behavioral;
```

VHDL Selection – when-else

- when-else - example