VHDL Selection – with-select

- with-select
  - Choose a value when a certain situation exists

```
with decision_signal select result_signal <=        -- exhaustive list
      result_value when decision_value,
      result_value when decision_value,
      result_value when decision_value,
      result_value when decision_value;
```

Limitation: Only one result signal

VHDL Selection – with-select

- with-select
  - inA – 2 bit std_logic_vector

Exhaustive List

```
with inA select outA <=   "0100" when "01",
                          "0010" when "10",
                          "0001" when "11",
                          "1010" when "00",
                          "0000" when others;
```

Partial List

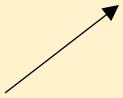
```
with inA select outA <=   "0100" when "01",
                          "0010" when "10",
                          "0000" when others;
```

Partially Common Result

```
with inA select outA <=   "0100" when "01",
                          "0010" when "10",
                          "0001" when ("11" or "00"),
                          "0000" when others;
```


Complex Selection

```
with (inA and inB) select outA <= "0100" when "01",
                                  "0010" when "10",
                                  "0001" when "00",
                                  "0000" when others;
```



VHDL Selection – with-select

- with-select
  - inA – 2 bit std_logic_vector

Exhaustive List

```
with inA select outA <=   sig1 when "01",
                          sig2 when "10",
                          sig3 when "11",
                          sig4 when "00",
                          sigx when others;
```

Partial List

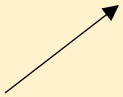
```
with inA select outA <=   sig1 when "01",
                          sig2 when "10",
                          sigx when others;
```

Partially Common Result

```
with inA select outA <=   sig1 when "01",
                          sig2 when "10",
                          sig3 when ("11" or "00"),
                          sigx when others;
```


Complex Selection

```
with (inA and inB) select outA <=sig1 when "01",
                                 sig2 when "10",
                                 sig3 when "00",
                                 sigx when others;
```



VHDL Selection – with-select

- with-select - example

```
----------------------------------------
--
-- with_select_example.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
----------------------------------------
--
-- with-select example
--
----------------------------------------
--
-- Inputs: inC
-- Outputs: outV
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity with_select_example is
   port (
         i_inC:   in std_logic_vector(3 downto 0);
         o_outV: out std_logic_vector(3 downto 0)
   );
end entity;
```

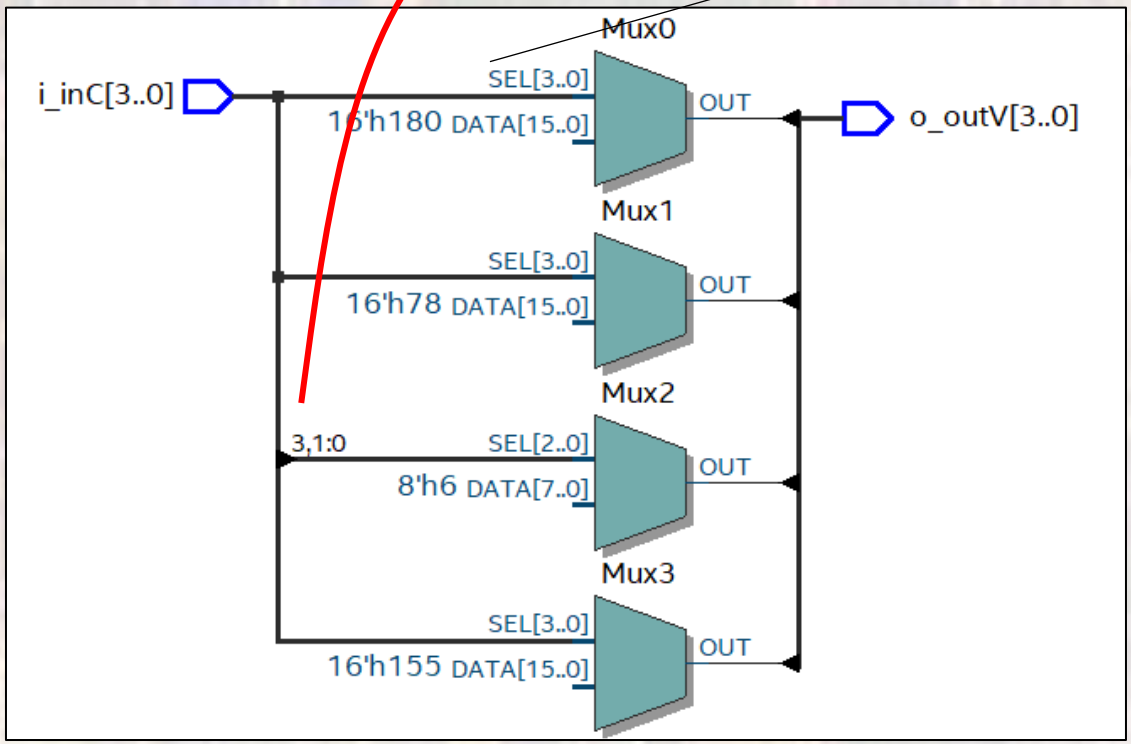
```
architecture behavioral of with_select_example is

begin
   with i_inC select o_outV <=
      "0001" when "0000",
      "0010" when "0001",
      "0011" when "0010",
      "0100" when "0011",
      "0101" when "0100",
      "0110" when "0101",
      "0111" when "0110",
      "1000" when "0111",
      "1001" when "1000",
      "0000" when others;

end behavioral;
```

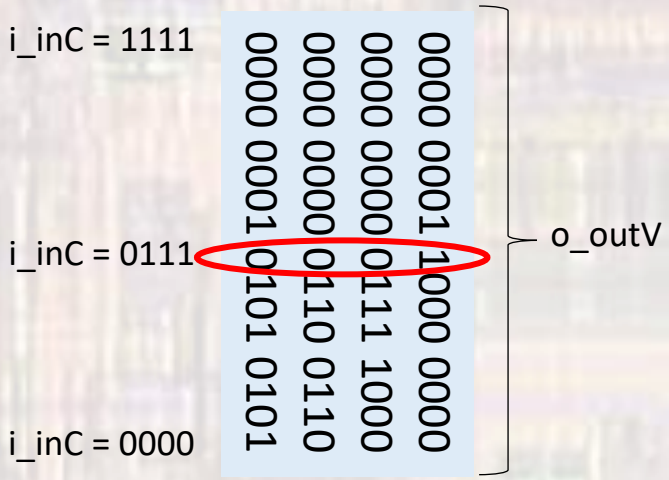
VHDL Selection – with-select

- with-select - example

Mux0 0000 0001 1000 0000
0000 0000 0111 1000
0000 0000 0110 0110
Mux3 0000 0001 0101 0101

complex wiring






```
"1000" when "0111",
"1001" when "1000"
```

Note: mux numbering does not correlate to bit numbering