ADC14 Info Sheet

x= 0:31

ADC14	->	CTL0	Control reg 0
		CTL1	Control reg 1
		LO0	Threshold Low - low
		HI0	Threshold Low - high
		LO1	Threshold High - low
		HI1	Threshold High - high
		MCTL[x]	Memory Control Registers
		MEM[x]	Memory registers
		IER0	Interrupt Enable reg 0
		IER1	Interrupt Enable reg 1
		IFGR0	Flag reg 0
		IFGR1	Flag reg 1
		CLRIFGR0	Clear Flag reg 0
		CLRIFGR1	Clear Flag reg 1
		IV	Interrupt Vector

ADC14_IRQHandler INTISR[24] ADC14 IFG[0-31], LO/IN/HI-IFG, RDYIFG, OVIFG, TOVIFG

PORT			DIR	PSEL[1:0]		PORT			DIR	PSEL[1:0]
P5.5	A	0		11		P4.1	A	12		11
P5.4	A	1		11		P4.0	A	13		11
P5.3	A	2		11		P6.1	A	14		11
P5.2	A	3		11		P6.0	A	15		11
P5.1	A	4		11		P9.1	A	16		11
P5.0	A	5		11		P9.0	A	17		11
P4.7	A	6		11		P8.7	A	18		11
P4.6	A	7		11		P8.6	A	19		11
P4.5	A	8		11		P8.5	A	20		11
P4.4	A	9		11		P8.4	A	21		11
P4.3	A	10		11		P8.3	A	22		11
P4.2	A	11		11		P8.2	A	23		11