Bit Banding Example

Last updated 6/18/18

Bit Banding Example

Set the Timer32 enable bit using bit-banding

Bit Band offset – 0x4200 000

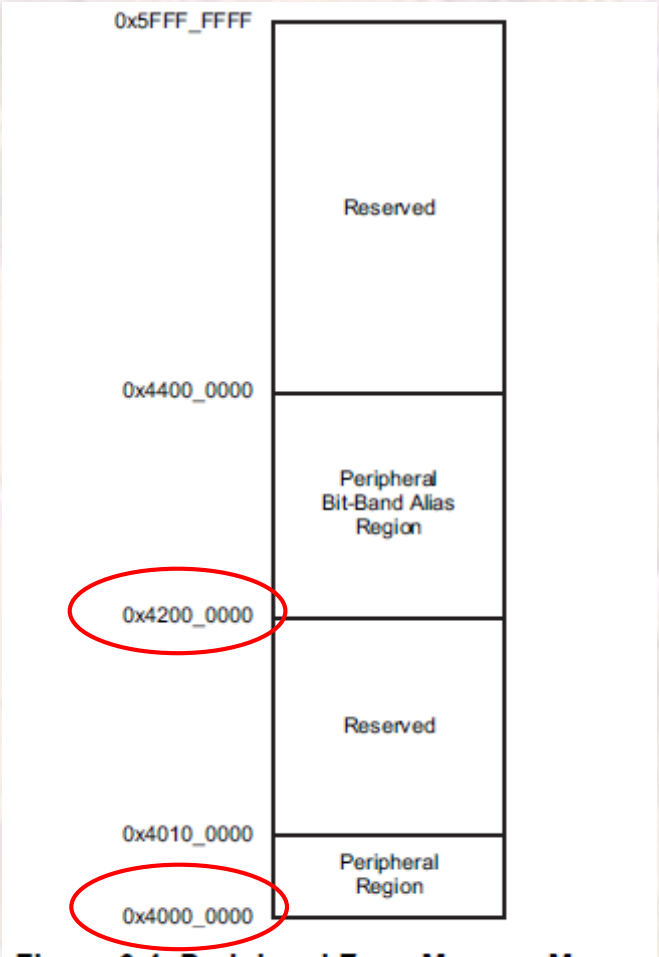


Figure 6-4. Peripheral Zone Memory Map

Bit Banding Example

Set the Timer32 enable bit using bit-banding

Peripheral (Timer32) offset
- 0xC000

Table 6-1. Peripheral Address Offsets

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_0000–0x4000_03FF	Timer_A0	Table 6-2	16-bit peripheral
0x4000_0400–0x4000_07FF	Timer_A1	Table 6-3	16-bit peripheral
0x4000_0800–0x4000_0BFF	Timer_A2	Table 6-4	16-bit peripheral
0x4000_0C00–0x4000_0FFF	Timer_A3	Table 6-5	16-bit peripheral
0x4000_1000–0x4000_13FF	eUSCI_A0	Table 6-6	16-bit peripheral
0x4000_1400–0x4000_17FF	eUSCI_A1	Table 6-7	16-bit peripheral
0x4000_1800–0x4000_1BFF	eUSCI_A2	Table 6-8	16-bit peripheral
0x4000_1C00–0x4000_1FFF	eUSCI_A3	Table 6-9	16-bit peripheral
0x4000_2000–0x4000_23FF	eUSCI_B0	Table 6-10	16-bit peripheral
0x4000_2400–0x4000_27FF	eUSCI_B1	Table 6-11	16-bit peripheral
0x4000_2800–0x4000_2BFF	eUSCI_B2	Table 6-12	16-bit peripheral
0x4000_2C00–0x4000_2FFF	eUSCI_B3	Table 6-13	16-bit peripheral
0x4000_3000–0x4000_33FF	REF_A	Table 6-14	16-bit peripheral
0x4000_3400–0x4000_37FF	COMP_E0	Table 6-15	16-bit peripheral
0x4000_3800–0x4000_3BFF	COMP_E1	Table 6-16	16-bit peripheral
0x4000_3C00–0x4000_3FFF	AES256	Table 6-17	16-bit peripheral
0x4000_4000–0x4000_43FF	CRC32	Table 6-18	16-bit peripheral
0x4000_4400–0x4000_47FF	RTC_C	Table 6-19	16-bit peripheral
0x4000_4800–0x4000_4BFF	WDT_A	Table 6-20	16-bit peripheral
0x4000_4C00–0x4000_4FFF	Port Module	Table 6-21	16-bit peripheral
0x4000_5000–0x4000_53FF	Port Mapping Controller	Table 6-22	16-bit peripheral
0x4000_5400–0x4000_57FF	Capacitive Touch I/O 0	Table 6-23	16-bit peripheral
0x4000_5800–0x4000_5BFF	Capacitive Touch I/O 1	Table 6-24	16-bit peripheral
0x4000_5C00–0x4000_8FFF	Reserved		Read only, always reads 0h
0x4000_9000–0x4000_BFFF	Reserved		Read only, always reads 0h
0x4000_C000–0x4000_CFFF	Timer32	Table 6-25	
0x4000_D000–0x4000_DFFF	Reserved		Read only, always reads 0h
0x4000_E000–0x4000_FFFF	DMA	Table 6-26	
0x4001_0000–0x4001_03FF	PCM	Table 6-27	
0x4001_0400–0x4001_07FF	CS	Table 6-28	
0x4001_0800–0x4001_0FFF	PSS	Table 6-29	
0x4001_1000–0x4001_17FF	FLCTL	Table 6-30	
0x4001_1800–0x4001_1BFF	Reserved		Read only, always reads 0h
0x4001_1C00–0x4001_1FFF	Reserved		Read only, always reads 0h
0x4001_2000–0x4001_23FF	ADC14	Table 6-31	
0x4001_2400–0x4001_FFFF	Reserved		Read only, always reads 0h

Bit Banding Example

Set the Timer32 enable bit using bit-banding

Register offset – 0x08

Table 16-1. Timer32 Registers

Offset	Acronym	Register Name	Type	Reset	Section
00h	T32LOAD1	Timer 1 Load Register	RW	0h	Section 16.5.1
04h	T32VALUE1	Timer 1 Current Value Register	R	FFFFFFFFh	Section 16.5.2
08h	T32CONTROL1	Timer 1 Timer Control Register	RW	20h	Section 16.5.3
0Ch	T32INTCLR1	Timer 1 Interrupt Clear Register	W	-	Section 16.5.4
10h	T32RIS1	Timer 1 Raw Interrupt Status Register	R	0h	Section 16.5.5
14h	T32MIS1	Timer 1 Interrupt Status Register	R	0h	Section 16.5.6
18h	T32BGLOAD1	Timer 1 Background Load Register	RW	0h	Section 16.5.7
20h	T32LOAD2	Timer 2 Load Register	RW	0h	Section 16.5.8
24h	T32VALUE2	Timer 2 Current Value Register	R	FFFFFFFFh	Section 16.5.9
28h	T32CONTROL2	Timer 2 Timer Control Register	RW	20h	Section 16.5.10
2Ch	T32INTCLR2	Timer 2 Interrupt Clear Register	W	X	Section 16.5.11
30h	T32RIS2	Timer 2 Raw Interrupt Status Register	R	0h	Section 16.5.12
34h	T32MIS2	Timer 2 Interrupt Status Register	R	0h	Section 16.5.13
38h	T32BGLOAD2	Timer 2 Background Load Register	RW	0h	Section 16.5.14

Bit Banding Example

Set the Timer32 enable bit using bit-banding

Bit offset – 0x07

Figure 16-4. T32CONTROL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ENABLE	MODE	IE	Reserved	PRESCALE		SIZE	ONESHOT
r-0								rw-0	rw-0	rw-1	r-0	rw-0		rw-0	rw-0

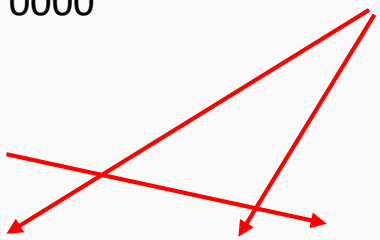
Bit Banding Example

Set the Timer32 enable bit using bit-banding

```
// Peripheral base address is 0x4000 0000
// Peripheral bit band base address is 0x4200 0000
// Timer32 offset is 0xC000
// Register offset is 0x08
// bit offset is 4bytes * bit# = 0x04 * 7 = 0x1C

// Bitband alias --> 0x4200 0000 + 0x20*0xC000 + 0x20*0x08 + 0x1C = 0x4218 011C
```

each byte address needs to allow
for 8 bits * 4 bytes = 32 bit-band-bytes



```
//Solution 1
//
// Define a pointer to use to access memory
volatile uint8_t * T32_en_ptr;
T32_en_ptr = (volatile uint8_t *)(0x4218011C);  // need to cast the integer

// set the initial value for the output
*T32_en_ptr = 0;

*T32_en_ptr = 1;

*T32_en_ptr = 0;
```

```
//Solution 2
//
// Define an alias to use to access memory
#define T32_en (*((volatile uint8_t *)(0x4218011C)))

// set the initial value for the output
T32_en = 0;

T32_en = 1;

T32_en = 0;
```

Cast the value as a pointer to an 8 bit int because the processor ignores all bits but bit0 on writes, and returns 1 byte of either 0x00 or 0x01 on reads

Bit Banding Example

Set the Timer32 enable bit using bit-banding

Debug – single step