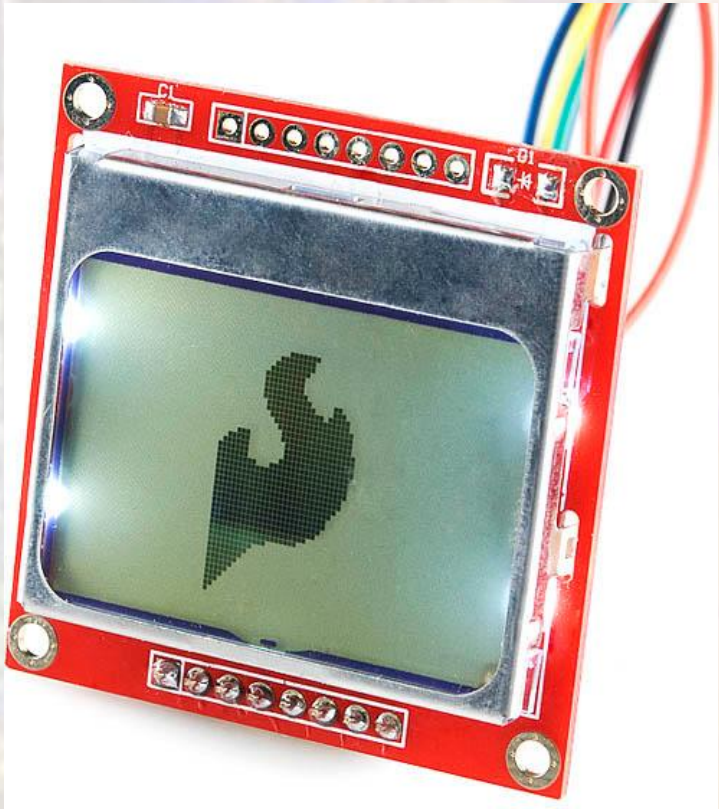
LCD Guide

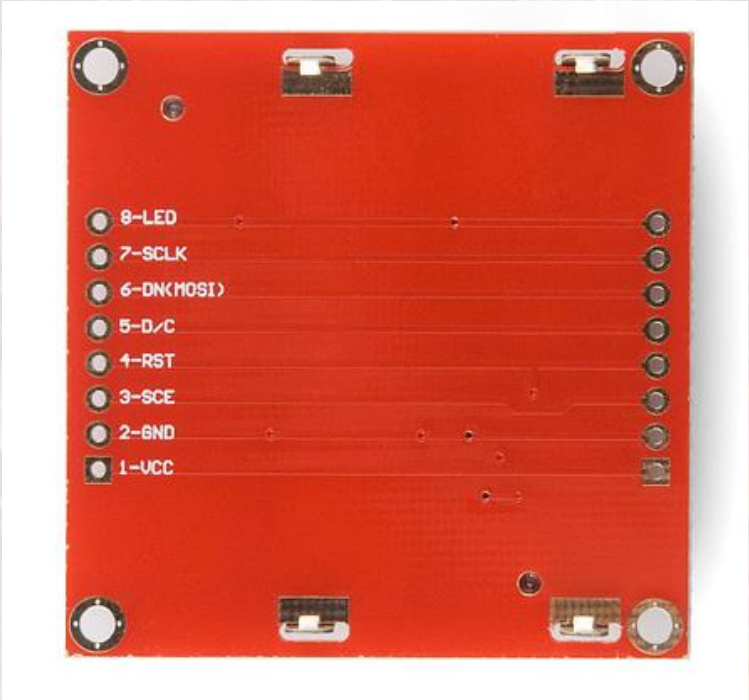
Last updated – 11/22/21

LCD Guide

- Nokia 5110 LCD Display
  - Originally used in Nokia phones



src: Sparkfun



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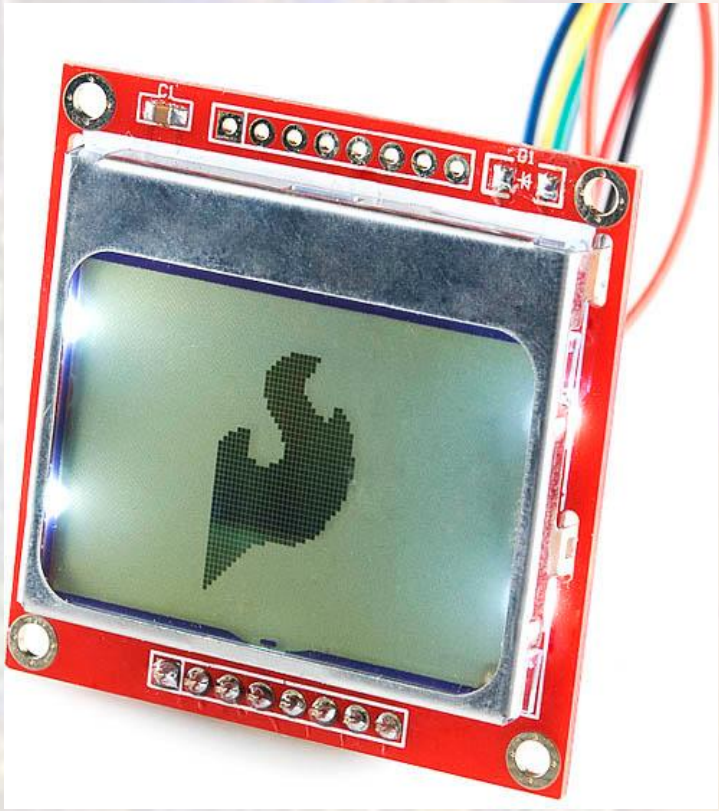
- Nokia 5110 LCD Display
  - Blue version



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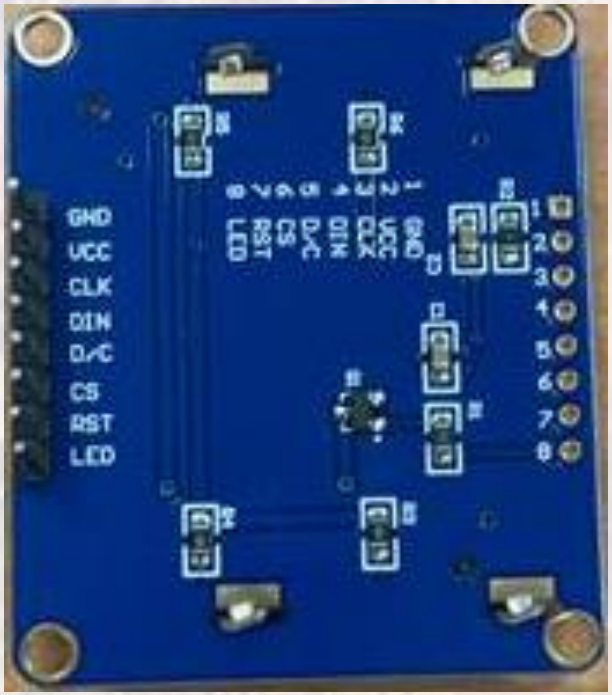


LCD Guide

- Nokia 5110 LCD Display
  - 2 Primary Components
  - 48 x 84 monochrome LCD display
    - The actual display
    - 4 backlight LEDs
  - Phillips PCD8544 LCD Driver/Controller
    - Drives the required LCD signals
    - Contains a Display Data RAM (DDRAM) to hold the desired display data
    - SPI interface (from the controller)

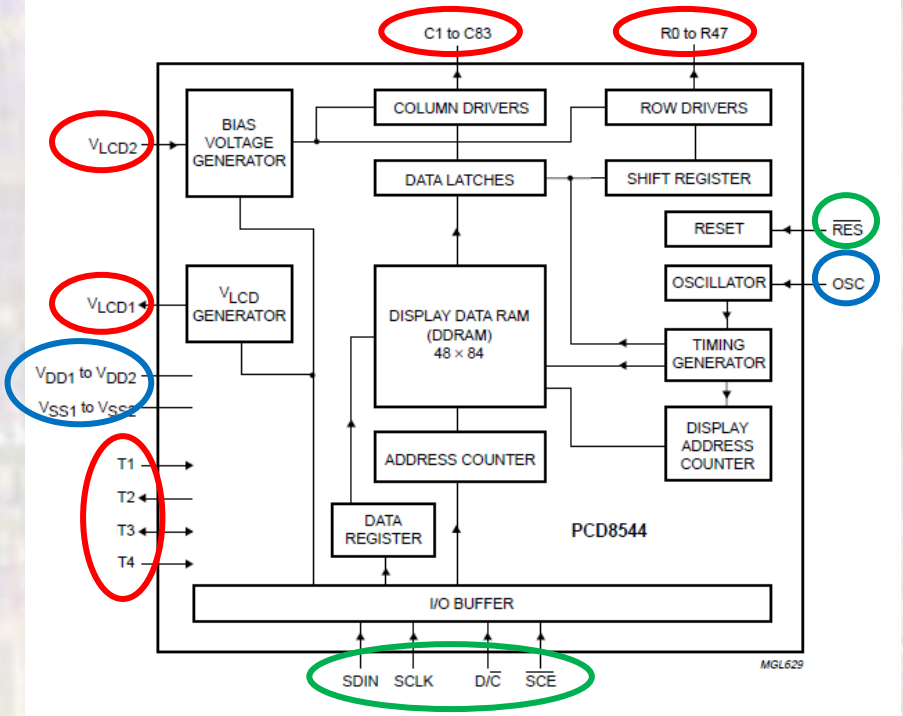
LCD Guide

- Nokia 5110 LCD Display
  - Phillips PCD8544 LCD Driver/Controller

to/from LCD

to/from uC

to/from Board



SYMBOL	DESCRIPTION
R0 to R47	LCD row driver outputs
C0 to C83	LCD column driver outputs
V_{SS1}, V_{SS2}	ground
V_{DD1}, V_{DD2}	supply voltage
V_{LCD1}, V_{LCD2}	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 input/output
T4	test 4 input
SDIN	serial data input
SCLK	serial clock input
D/$\overline{C}$	data/$\overline{\text{command}}$
$\overline{SCE}$	chip enable
OSC	oscillator
$\overline{RES}$	external reset input
dummy1, 2, 3, 4	not connected

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- Nokia 5110 LCD Display
  - Phillips PCD8544 LCD Driver/Controller
  - Simplified Operation
    - Configure the controller and LCD by sending “commands” to the controller
    - Transmit data to the controller for storage in the DDRAM
    - The controller creates all the signals necessary to continuously write the data from the DDRAM to the display
      - Writes are fast enough the human eye cannot see any flicker
    - See the PCD8544 spec for additional details

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- Phillips PCD8544 LCD Driver/Controller
  - Commands
  - D/C signal = 1
    - Indicates data is being transmitted
    - Data is saved in the DDRAM
  - D/C signal = 0
    - Indicates a command is being transmitted
    - Configure the LCD
    - Set the X and Y location for the DDRAM

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INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								DESCRIPTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
(H = 0 or 1)										
NOP	0	0	0	0	0	0	0	0	0	no operation
Function set	0	0	0	1	0	0	PD	V	H	power down control; entry mode; extended instruction set control (H)
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to display RAM
(H = 0)										
Reserved	0	0	0	0	0	0	1	X	X	do not use
Display control	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	1	X	X	X	X	do not use
Set Y address of RAM	0	0	1	0	0	0	Y_2	Y_1	Y_0	sets Y-address of RAM; $0 \le Y \le 5$
Set X address of RAM	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X-address part of RAM; $0 \le X \le 83$
(H = 1)										
Reserved	0	0	0	0	0	0	0	0	1	do not use
	0	0	0	0	0	0	0	1	X	do not use
Temperature control	0	0	0	0	0	0	1	TC_1	TC_0	set Temperature Coefficient (TC_x)
Reserved	0	0	0	0	0	1	X	X	X	do not use
Bias system	0	0	0	0	1	0	BS_2	BS_1	BS_0	set Bias System (BS_x)
Reserved	0	0	1	X	X	X	X	X	X	do not use
Set V_{OP}	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

BIT	0	1
PD	chip is active	chip is in Power-down mode
V	horizontal addressing	vertical addressing
H	use basic instruction set	use extended instruction set
D and E		
00	display blank	
10	normal mode	
01	all display segments on	
11	inverse video mode	
TC_1 and TC_0		
00	V_{LCD} temperature coefficient 0	
01	V_{LCD} temperature coefficient 1	
10	V_{LCD} temperature coefficient 2	
11	V_{LCD} temperature coefficient 3	

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- SPI interface
  - We will cover the SPI interface later in the quarter

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- Circuit Configuration

Use SPI block in eUSCI on PORT 9

SCLK	P9.5	output
STE	P9.4	output
MISO	P9.7	output
~~MOSI~~	~~P9.6~~	unused

Use remaining GPIOs from PORT 9

D/C	P9.2	output
RST	P9.3	output
	note this is active low	

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- Circuit Configuration
  - Blue version

GND
3.3V
SPI - SCLK
SPI – MISO (Tx)
GPIO – D/C
SPI – STE (Chip Select)
GPIO - resetBAR
Backlight (N/C)

Use SPI block in eUSCI on PORT 9

SCLK	P9.5	output
STE	P9.4	output
MISO	P9.7	output
~~MOSI~~	~~P9.6~~	unused

Use remaining GPIOs from PORT 9

D/C	P9.2	output
RST	P9.3	output
	note this is active low	

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- PORT Configuration

```
// LCD / SPI Port mapping
// P9.7 – MOSI, P9.5 – SCLK, P9.4 – CS(Chip Select), P9.3 – RST, P9.2 – D/C

P9->SEL0 |= 0xB0;          // 1x11 xxxx    P9.7, P9.5, and P9.4 as eUSCI (01) mode
P9->SEL1 &= ~0xB0;         // automatically set to outputs

P9->SEL0 &= ~0x0C;         // xxxx 00xx    P9.3 and P9.2 as GPIO (00) mode
P9->DIR |= 0x0C;           // xxxx 11xx    P9.3 and P9.2 outputs
```

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- SPI Configuration

Figure 22-12. UCAxCTLW0 Register

15	14	13	12	11	10	9	8
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCMODEx		UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
Modify only when UCSWRST = 1							

```
// SPI Configuration
// P9.7 – MOSI, P9.5 – SCLK, P9.4 – CS

EUSCI_A3->CTLW0 = 0x0001;          // sw reset activated
EUSCI_A3->CTLW0 = 0xAD83;          // 1010 ckph=1, ckpl=0, MSB first, 8 bit data
                                   // 1101 master, active low enable, synchronous
                                   // 10xx clock=SMCLK
                                   // xx11 CS active, SW reset activated
```

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- SPI Configuration

Figure 22-14. UCAxBRW Register

15	14	13	12	11	10	9	8
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Modify only when UCSWRST = 1

// With a 48MHz HFXTCLK clock – set SCLK to 4MHz for PCD8544
EUSCI_A3->BRW = 0x03; // 48MHz/4→16MHz SMCLK /4 →4MHz SCLK

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- SPI Configuration

Figure 22-15. UCAxMCTLW Register

15	14	13	12	11	10	9	8
UCBRSx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
UCBRFx				Reserved			UCOS16
rw-0	rw-0	rw-0	rw-0	r0	r0	r0	rw-0

Modify only when UCSWRST = 1

```
// no modulation for SPI
EUSCI_A3->MCTLW = 0;
```

LCD Guide

- SPI Configuration

Figure 22-12. UCAxCTLW0 Register

15	14	13	12	11	10	9	8
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCMODEx		UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
Modify only when UCSWRST = 1							

EUSCI_A3->CTLW0 &= ~0x0001; // release SW reset

Figure 22-21. UCAxIE Register

15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved				UCTXCPTIE	UCSTTIE	UCTXIE	UCRXIE
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

EUSCI_A3->IE &= ~0x0003; // disable interrupt creation

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- Use MSOE_Lib to configure and operate the LCD

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- Alternate UART configuration
  - Provided for students who may have blown up one of the pins on the original UART

```
//////////////////////////////////////////////////////////////////
//
// Nokia 5110 LCD Module / MSP432 Hardware Configuration (pinout)
//       ***  Alternate UART  ***
//
// VCC                          3.3V
// GND                          GND
// SCE (Slave Select)           P2.0   output
// RST                          P1.6   output    Active LOW
// D/C (data/commandBar)        P1.7   output
// D/N (MOSI)                   P2.3   output
// SCLK                         P2.1   output
// LED (back light)             N/C
//
//////////////////////////////////////////////////////////////////
```

  - Use the *msoe_lib_lcd_alt_io.h* file include instead of the regular lcd library include
    - All functions use the same names