Logic Review

Common – last updated 3/4/19

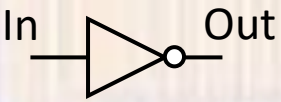
Logic Review

- Buffers

non-Inverting

In	Out
0	0
1	1

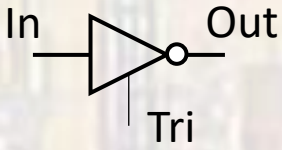
Inverting



In	Out
0	1
1	0

notA ~A A’

Tri-State



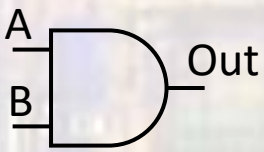
Tri	In	OUT
0	0	1
0	1	0
1	0	Z
1	1	Z

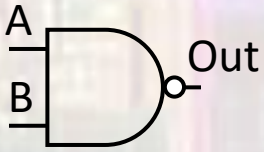
In	Tri	OUT
A	0	~A
X	1	Z

Logic Review

- Simple Gates

AND/NAND

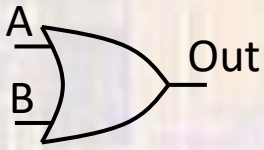


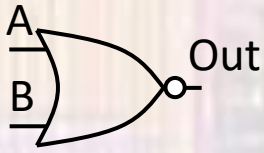


A	B	AND OUT	NAND OUT
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

A and B A nand B
A ^ B (A ^ B)'
A & B $\overline{A \& B}$
AB A*B

OR/NOR

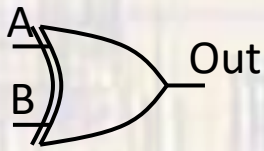


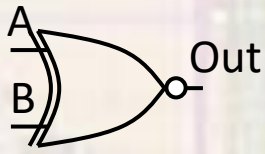


A	B	OR OUT	NOR OUT
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

A or B A nor B
A v B (A v B)'
A | B $\overline{A \mid B}$
A + B

XOR/XNOR





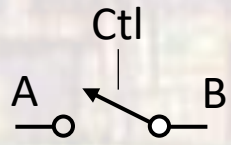
A	B	XOR OUT	XNOR OUT
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

A xor B A xnor B
$A \oplus B$ $(A \oplus B)'$

Logic Review

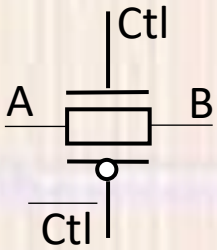
- Switches

Switch



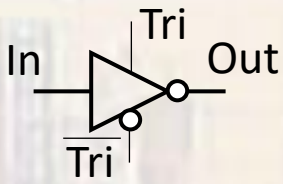
Ctl	State
0	X
1	A = B

Switch



Ctl	State
0	X
1	A = B

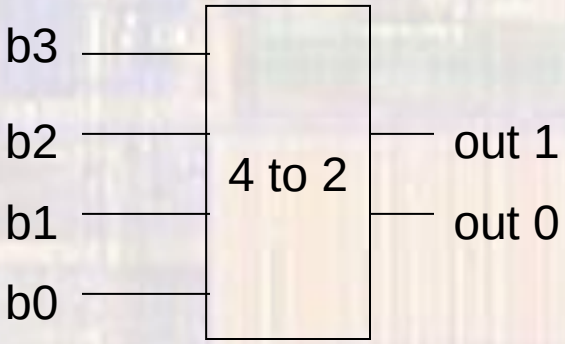
Tristate

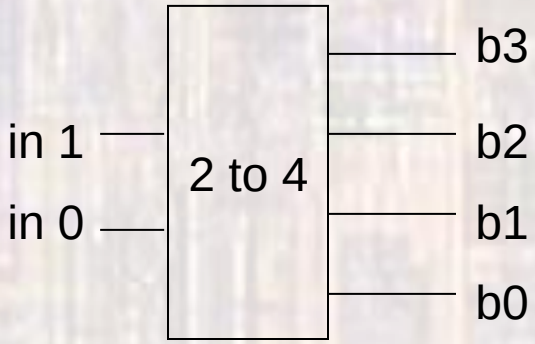


In	Tri	Tri bar	Out
A	0	0	U
A	0	1	A’
A	1	0	Z
A	1	1	U

Logic Review

- Coder / Decoder



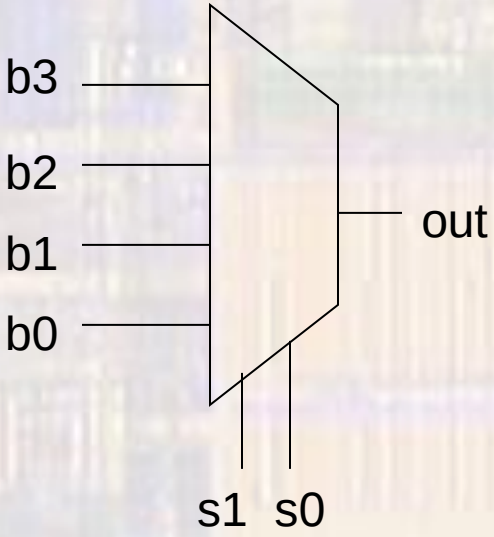


b3	b2	b1	b0	out 1	out 0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

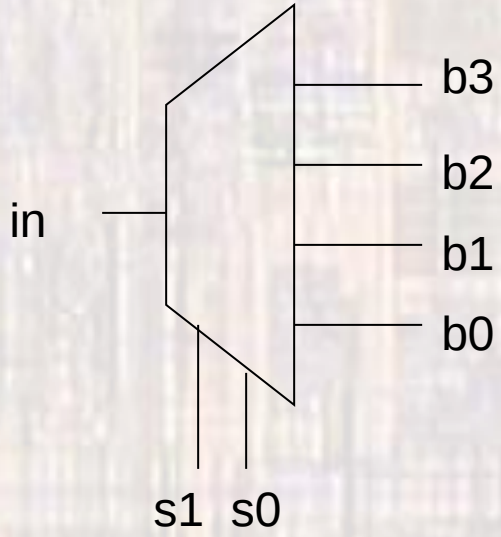
In 1	In 2	b3	b2	b1	b0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Logic Review

- Multiplexer/ Demultiplexer



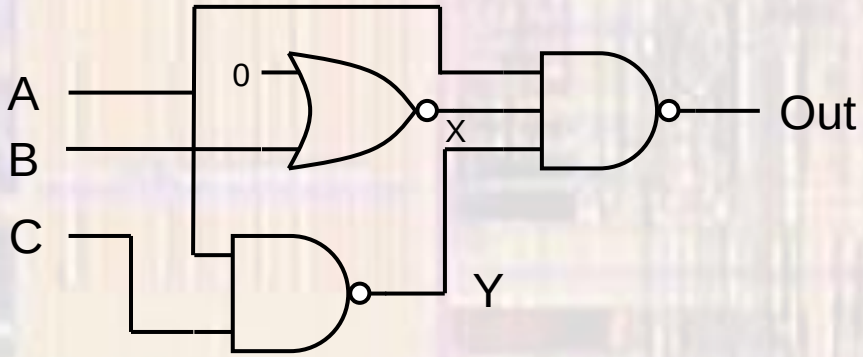
s1	S0	out
0	0	b0
0	1	b1
1	0	b2
1	1	b3



s1	s0	b3	b2	b1	b0
0	0	0	0	0	in
0	1	0	0	in	0
1	0	0	in	0	0
1	1	in	0	0	0

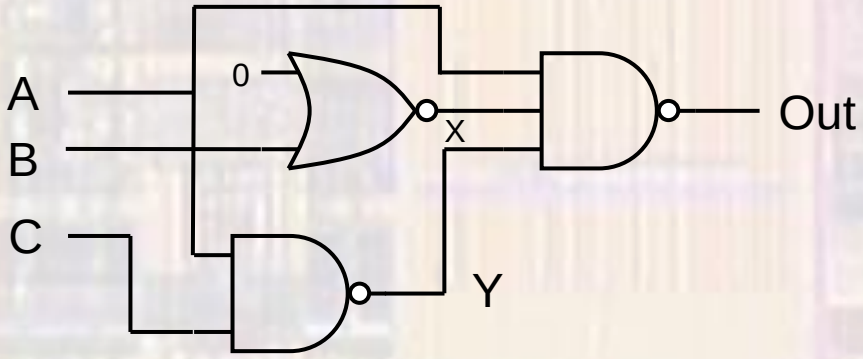
Logic Review

- Logic Analysis



Logic Review

- Logic Analysis



A	B	C	X	Y	Out
			(B+0)'	(AC)'	(AXY)'
0	0	0	1	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	0	1

Logic Review

- de Morgan's Laws

$$(A \cup B)' = A' \cap B' \qquad \overline{(A + B)} = \overline{A}\,\overline{B}$$

$$(A \cap B)' = A' \cup B' \qquad \overline{(AB)} = \overline{A} + \overline{B}$$

$$(A')' = A \qquad \overline{(\overline{A})} = A$$

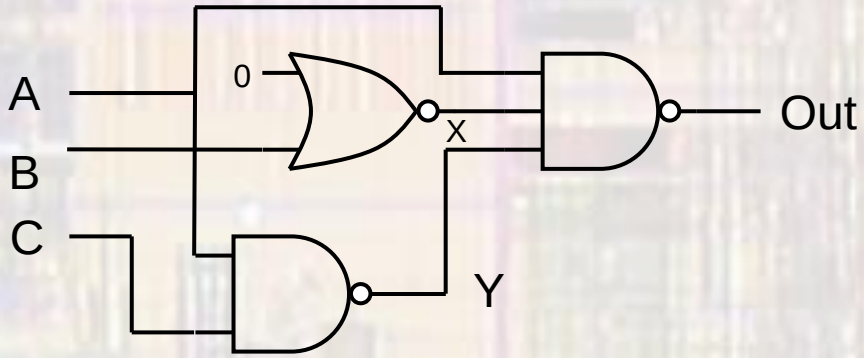
Logic Review

- de Morgan's Laws

$$(A \cup B)' = A' \cap B' \qquad \overline{(A + B)} = \overline{A}\,\overline{B}$$

$$(A \cap B)' = A' \cup B' \qquad \overline{(AB)} = \overline{A} + \overline{B}$$

$$(A')' = A \qquad \overline{(\overline{A})} = A$$

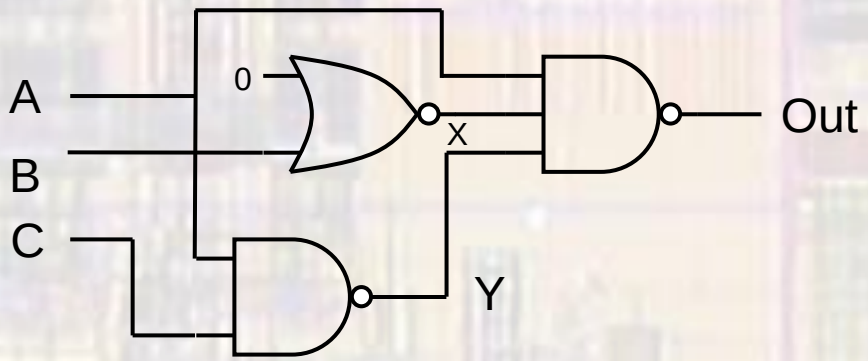


Logic Review

- de Morgan's Laws

$$(A \cup B)' = A' \cap B'$$
$$(A \cap B)' = A' \cup B'$$
$$(A')' = A$$

$$\overline{(A + B)} = \overline{A}\,\overline{B}$$
$$\overline{(AB)} = \overline{A} + \overline{B}$$
$$\overline{(\overline{A})} = A$$



Out = $\overline{AXY}$

$\overline{A(\overline{B+0})(\overline{AC})}$

$\overline{A} + (B+0) + (AC)$

$\overline{A} + B + AC$

Logic Review

- Sum-of-Products, Product-of-Sums

Sum-of-Products	$(A \cap B) \cup (C \cap D) \cup (E \cap F)$	$AB + CD + EF$
Product-of-Sums	$(A \cup B) \cap (C \cup D) \cap (E \cup F)$	$(A + B)(C + D)(E + F)$

Why ???

Logic Review

- minterm / maxterm

A	B	Y	minterm	maxterm
0	0	0	A'B'	A + B
0	1	1	A'B	A + B'
1	0	0	AB'	A' + B
1	1	1	AB	A' + B'

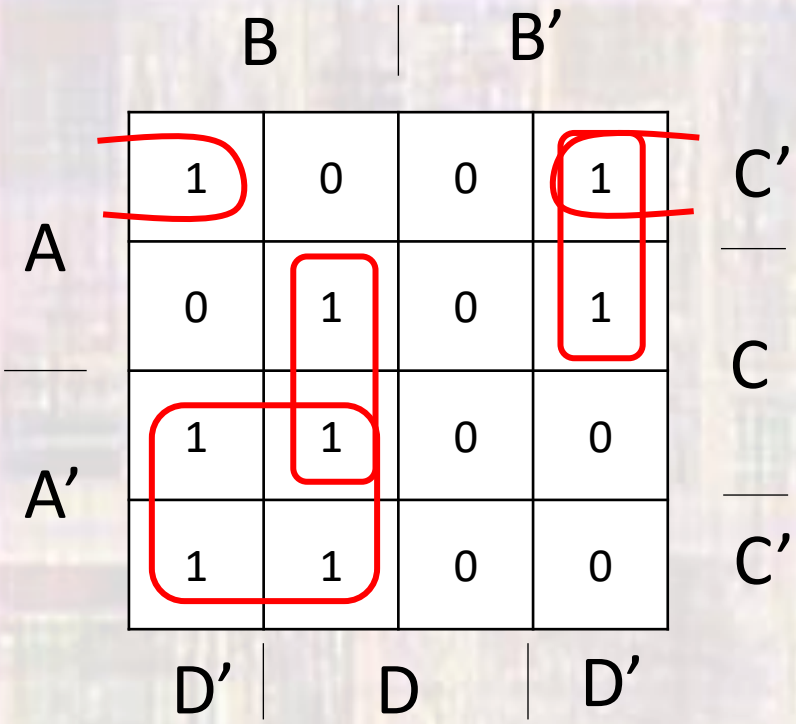
- SOP: Y = A'B + AB

- POS: Y = (A + B) (A' + B)

Logic Review

- Karnaugh Maps

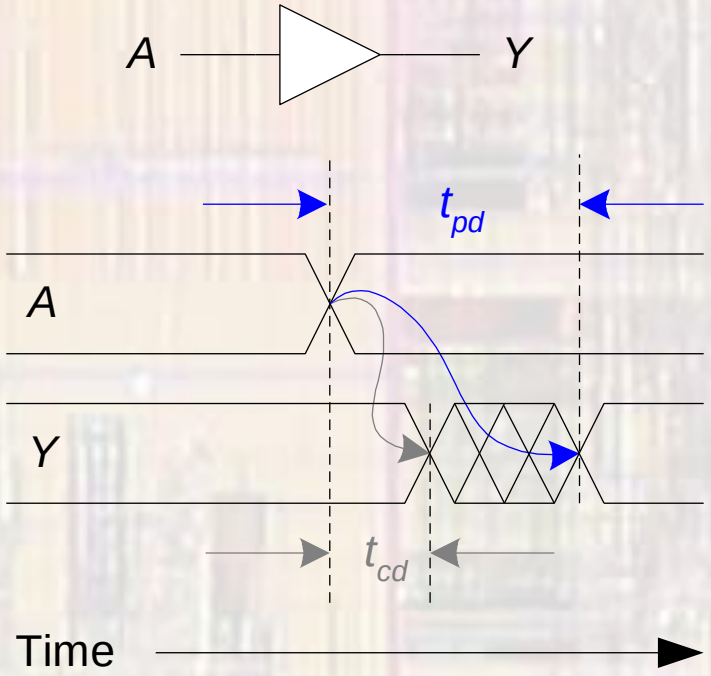
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



$A'B + BCD + AB'D' + AC'D'$

Logic Review

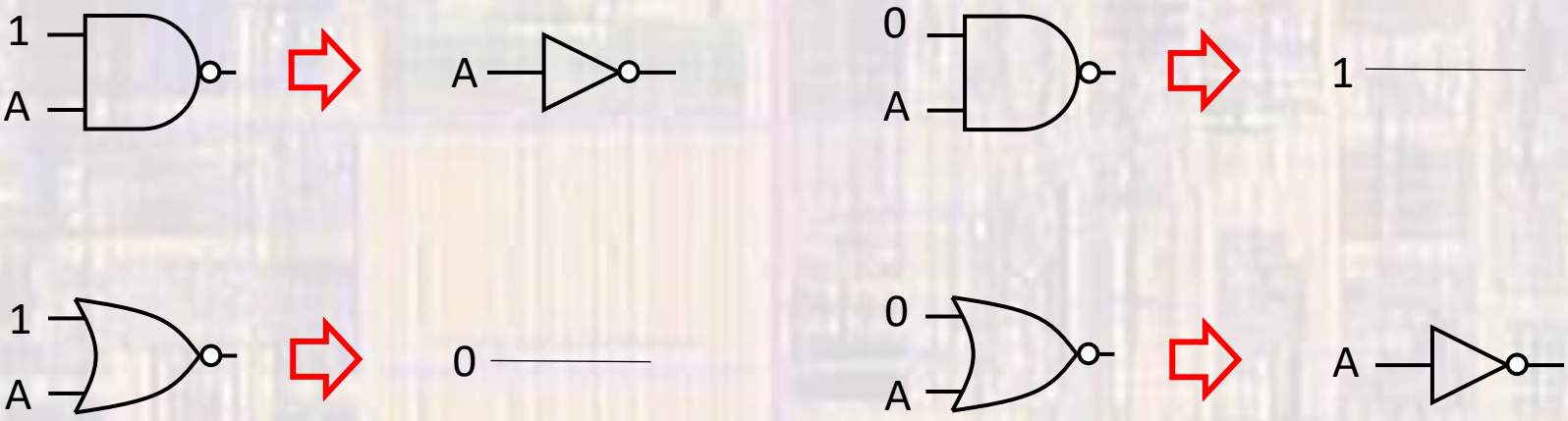
- Delays
  - t_{pd} = propagation delay
    - delay from input to valid output (max delay)
  - t_{cd} = contamination delay
    - delay from input to first movement on output (min delay)



src: Harris & Harris

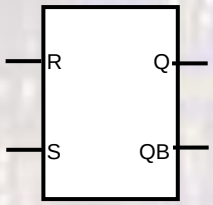
Logic Review

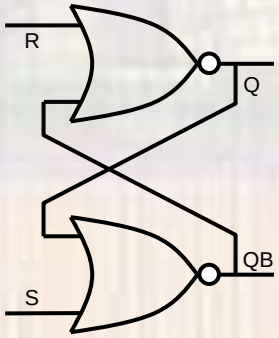
- Shortcuts

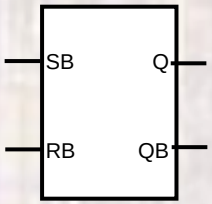


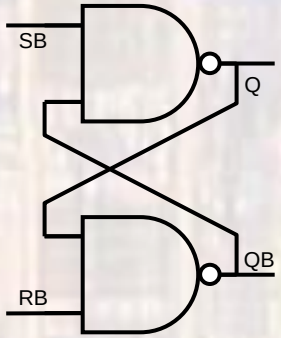
Logic Review

- Latches



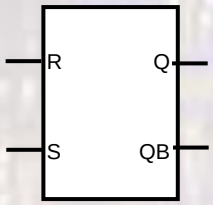


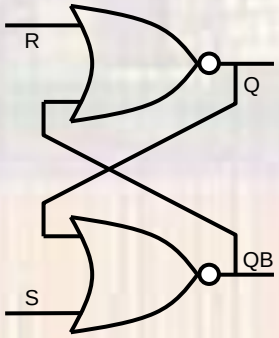




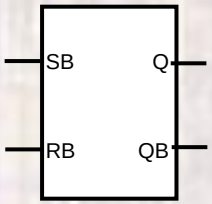
Logic Review

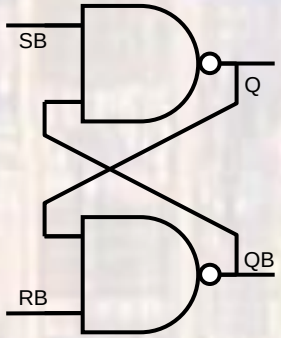
- Latches





S	R	Q	QB
0	0	No change	No change
0	1	0	1
1	0	1	0
1	1	0	0

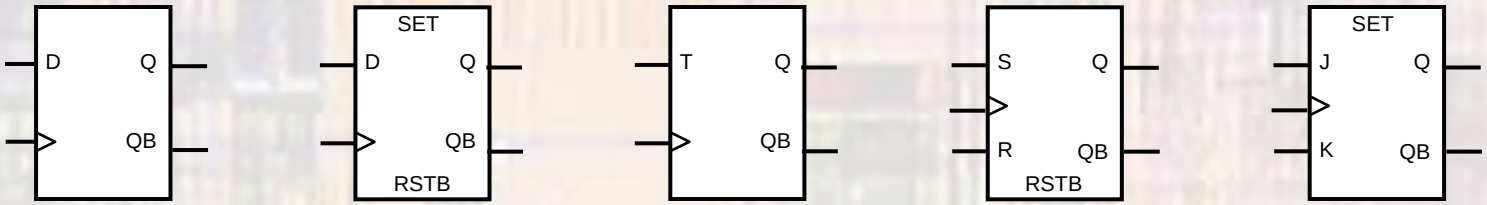




SB	RB	Q	QB
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No change	No change

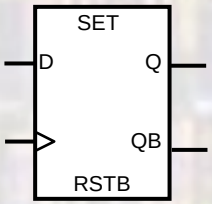
Logic Review

- Flip-Flops
  - Edge Triggered
    - Outputs only change on a rising or falling clock edge (synchronous)
    - Outputs depend on the state of the inputs at the clock edge
  - Some have asynchronous set or reset inputs



Logic Review

- Flip-Flops
  - Edge Triggered D Flip-Flop
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs

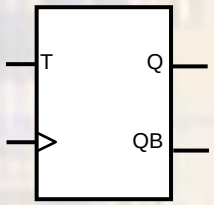


Set	Reset Bar	D		Q	QB
0	1	**0**		0	1
0	1	**1**		1	0
1	1	x		1	0
0	**0**	x		0	1

D at the rising clock edge

Logic Review

- Flip-Flops
  - Edge Triggered T Flip-Flop (Toggle)
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs



T		Q	QB
0		Q_{OLD}	QB_{OLD}
1		QB_{OLD}	Q_{OLD}

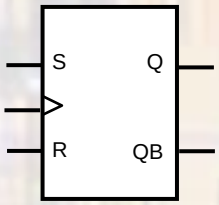
T at the rising clock edge

T		Q	QB
0		No Change	No Change
1		Toggle	Toggle

T at the rising clock edge

Logic Review

- Flip-Flops
  - Edge Triggered SR Flip-Flop (Set/Reset)
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs

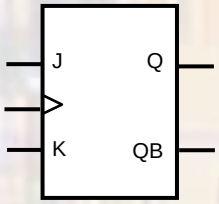


R	S		Q	QB
0	0		Q_{OLD}	QB_{OLD}
0	1		1	0
1	0		0	1
1	1		N/A	N/A

S,R at the rising clock edge

Logic Review

- Flip-Flops
  - Edge Triggered JK Flip-Flop
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs

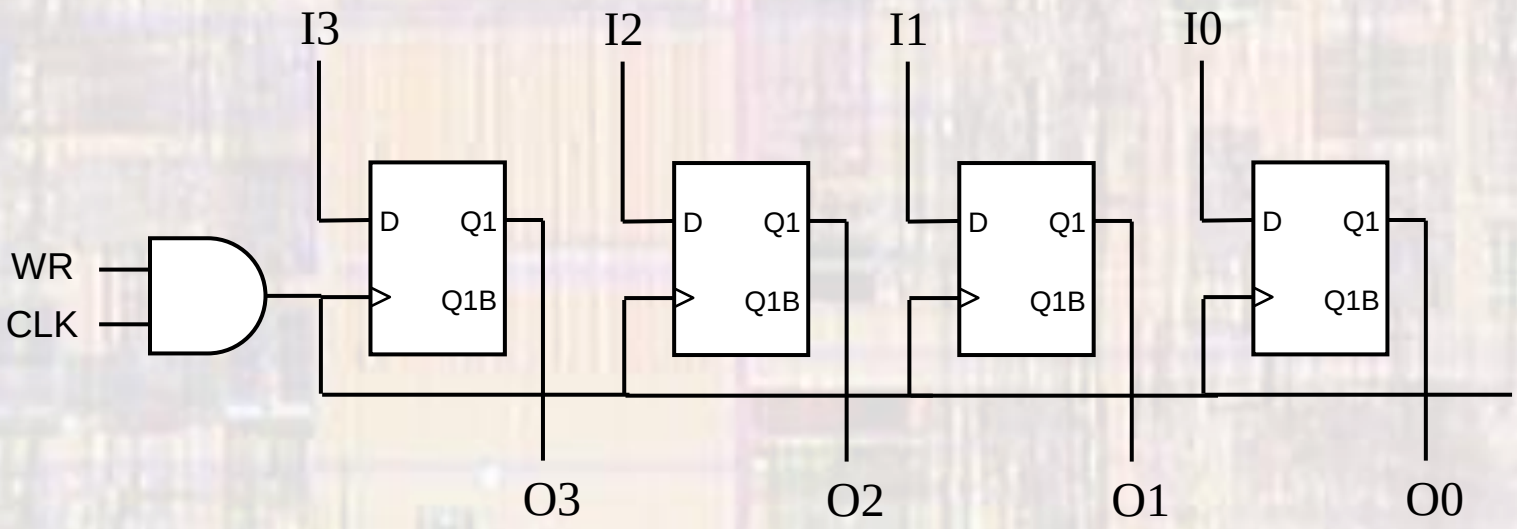


J	K		Q	QB
0	**0**		Q_{OLD}	QB_{OLD}
0	**1**		0	1
1	**0**		1	0
1	**1**		Toggle	Toggle

J,K at the rising clock edge

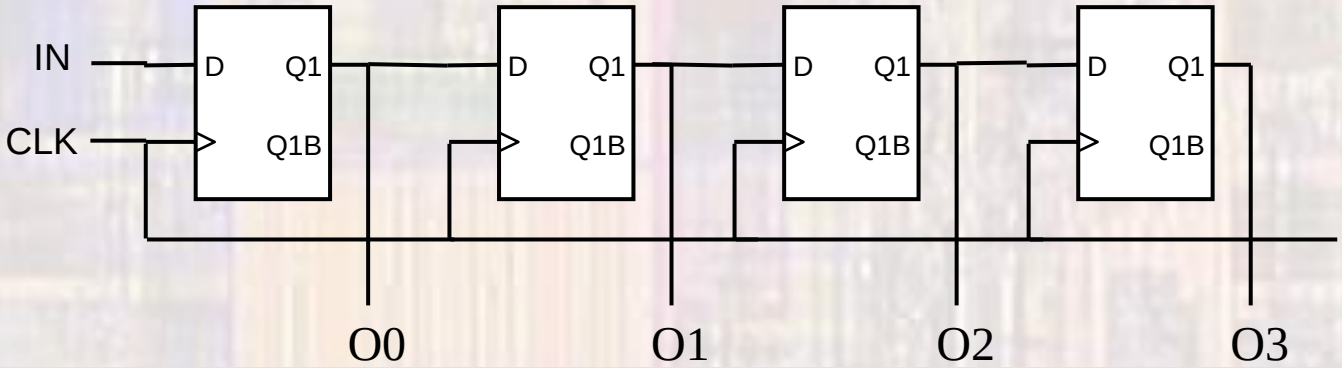
Logic Review

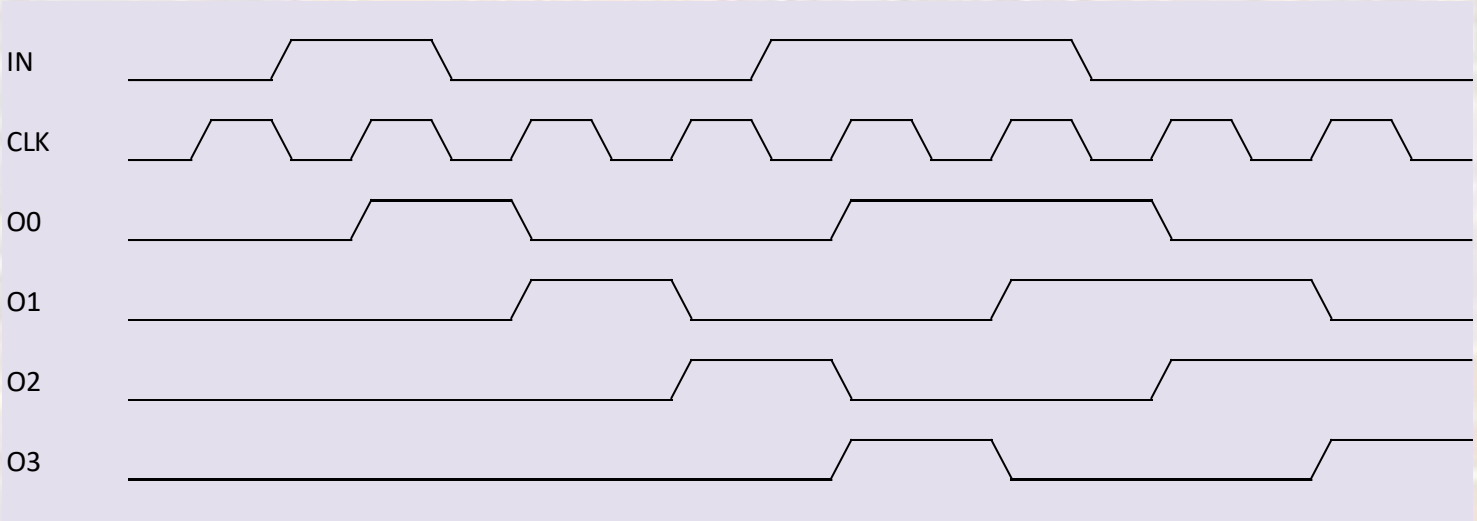
- Parallel Data Register



Logic Review

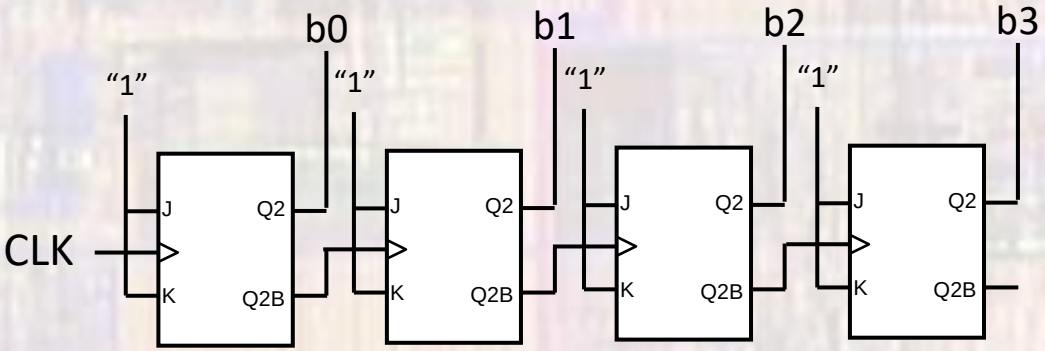
- Shift Register

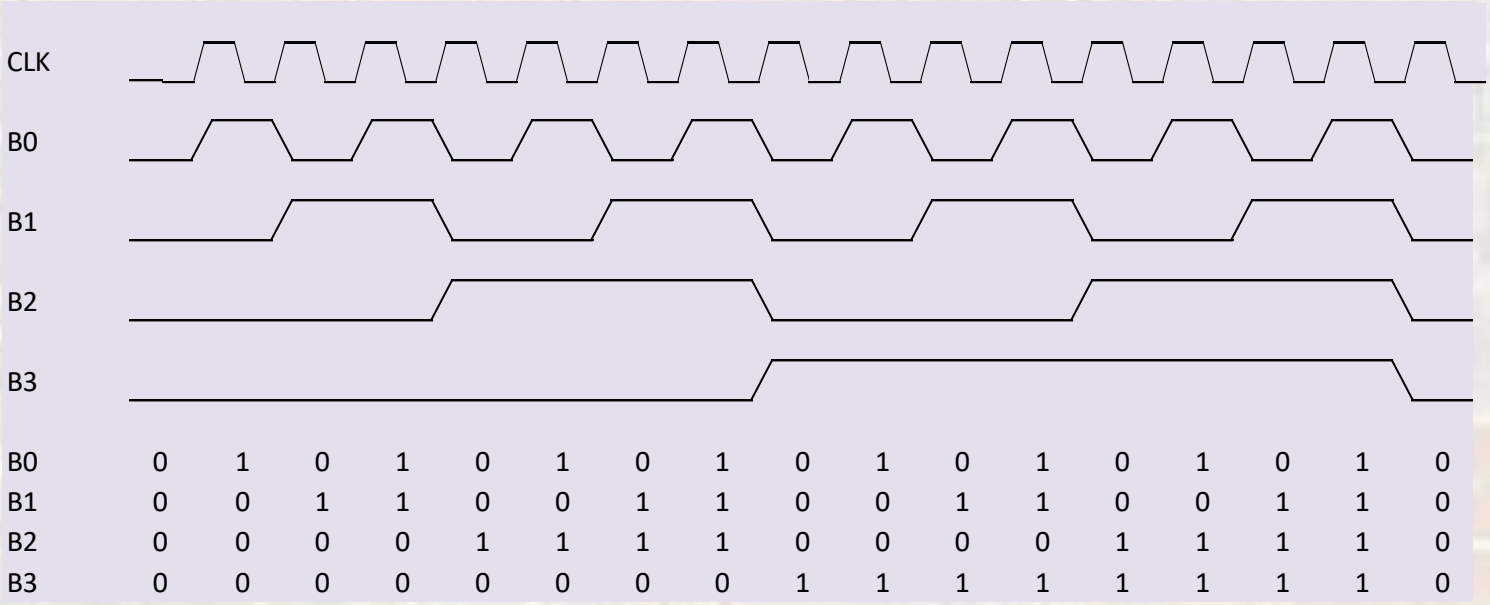




Logic Review

- Counter





B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0

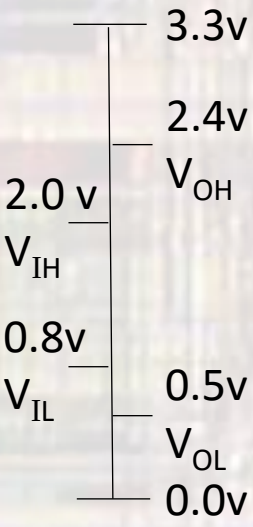
Logic Review

- Physical world
  - Voltage levels
    - System/Circuit dependent
    - Ideal:

3.3v System	‘1’ = 3.3v	‘0’ = 0.0v
1.8v System	‘1’ = 1.8v	‘0’ = 0.0v
1.2v System	‘1’ = 1.2v	‘0’ = 0.0v

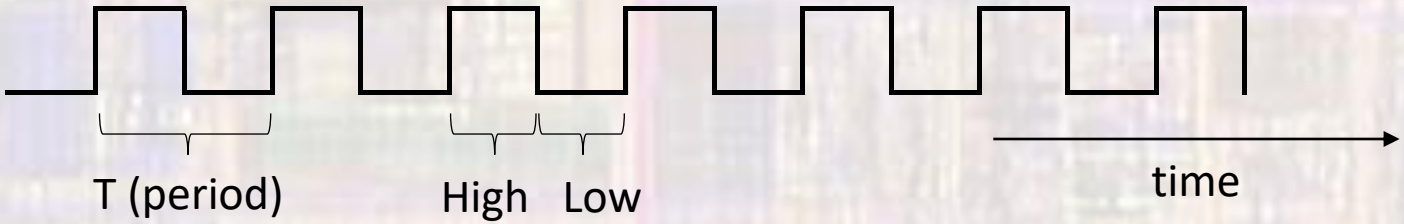
    - Real world:

3.3v System



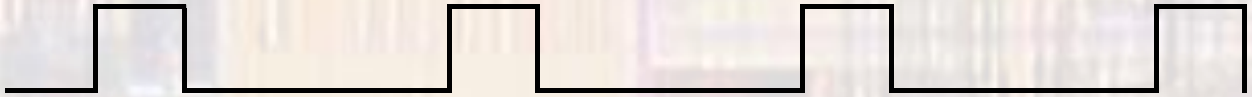
Logic Review

- Clock Systems

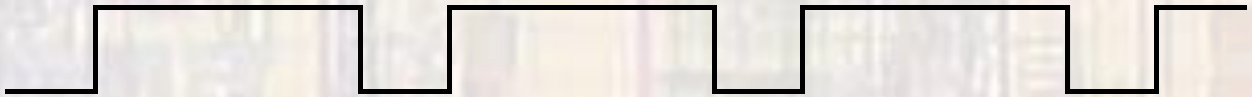


F (frequency) = 1/T Duty Cycle = High / T

50MHz <-> 20nS High = 10ns, Low = 10ns



25% duty cycle, 12.5Mhz



75% duty cycle, 12.5MHz