### Common - last updated 3/9/20

Test Bench Concept



- Example: Counter 4bit
  - Create 4-b counter HDL

```
--Proiect Header---
 -- counter_4bit.vhdl
-- Created: 2/23/18
 -- By: johnsontimoj
 - For: CE1911
---Project Overview---
-- This project creates a binary counter
-- for the modelsim hdl example
--- Project Details ---
-- Inputs: rstb, clock
-- outputs: b0, b1, b2, b3
-- Library inclusion
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all:
entity counter_4bit is
   port( i_rstb: in
                        std_logic;
         i_clk:
                 in
                        std_logic;
                        std_logic_vector(3 downto 0)
         o_cnt:
                  out
   );
end entity;
```

```
architecture behavioral of counter_4bit is
-- Internal Signals
-- signal cnt_sig: unsigned(3 downto 0);
begin
-- Update Section
-- Update Section
-- process(i_clk, i_rstb)
begin
if (i_rstb ='0') then
cnt_sig <= (others => '0');-- reset
elsif (rising_edge(i_clk)) then
cnt_sig <= (cnt_sig + 1); -- count up
end if;
end process;
--
-- Output Section
--
o_cnt <= std_logic_vector(cnt_sig);</pre>
```

end architecture;

- Example: Counter 4bit
  - Create a test bench

| counter_4bit_tb.vhdl  | <pre>chitecture testbench of counter_4bit_tb is<br/>signal CLK: std_logic;<br/>signal RSTB: std_logic;</pre> |
|---|--|
| created: 1/26/18<br>by: johnsontimoj<br>rev: 0  | <pre>signal CNT: std_logic_vector(3 downto 0);</pre>   |
| testbench for 4 bit counter<br>of counter_4bit.vhdl<br>brute force implementation<br> | <pre>constant PER: time := 20 ns;</pre>  |
|   | Component prototype  |
|   | COMPONENT counter_4bit   |
| library ieee;<br>use ieee.std_logic_1164.all;   | (<br>i_rstb : IN STD_LOGIC;  |
| entity counter_4bit_tb is<br>no entry - testbench                                     | <pre>0_CIK : IN STD_LOGIC;<br/>0_cnt : OUT STD_LOGIC_vector(3 downto 0) );</pre>                             |
| end entity;   | END COMPONENT;   |
|   |  |

| Device  | under test   | : (DUT)   |
|---|--|---|
| DUT: coun<br>port m   | ter_4bit<br>iap(<br>i_rstb<br>i_clk<br>o_cnt<br>);                           | => RSTB,<br>=> CLK,<br>=> CNT                       |
| Test p  | rocesses   |   |
| clock<br>clock: pr<br>begin<br>CLK<br>wai<br>inf<br>end proce | process<br>ocess<br>t for PER/2<br>inite: loop<br>CLK <= not<br>loop;<br>SS; | - no sens list allowe<br>2;<br>CLK; wait for PER/2; |
| Reset<br>reset: pr<br>begin<br>RST<br>end proce               | process<br>ocess<br>B <= '0'; W<br>B <= '1'; W<br>ss reset;                  | - no sens list allowe<br>wait for 2*PER;<br>wait;   |
| Run Pr<br>No run  | ocess<br>process fo  | or this design                                      |
|   |  |   |

- Example: Counter 4 bit
  - Elaborate the design (create RTL)
    - Note: leave the main design as the top level block
    - Processing → Start → Start Analysis and Elaboration
  - Check the RTL
    - Tools → Netlist Viewers → RTL Viewer



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- Example: Counter 4 bit
  - Setup the test bench
    - Assignments → Settings → EDA Tool Settings → Simulation → Test Benches
      - : enter the test bench file
      - : select the end simulation time
      - : select File name ... and select the test bench file

| Category:                           | Device/Board  |
|-------------------------------------|---|
| General                             | Simulation  |
| Files                               | Specify options for generating output files for use with other EDA tools. |
| Libraries                           |   |
| V IP Settings                       | Tool name: ModelSim-Altera  |
| Design Templates                    | Run gate-level simulation automatically after compilation                 |
| ✓ Operating Settings and Conditions | EDA Netlist Writer settings   |
| Voltage                             | Eormat for output netlist: VHDL   Time scale: 100 us                      |
| ✓ Compilation Process Settings      | Output directory: simulation/modelsim                                     |
| Incremental Compilation             | Map illegal HDL characters     Enable glitch filtering                    |
| Design Entry/Synthesis              | Options for Power Estimation  |
| Simulation                          |   |
| Board-Level                         | Generate Value Change Dump (VCD) file script Script Settings              |
| ✓ Compiler Settings                 | Design instance name:   |
| VHDL Input                          |   |
| Default Parameters                  | More EDA Netlist Writer Settings  |
| TimeQuest Timing Analyzer           | NativeLink setting-   |
| Assembler                           | O None  |
| Design Assistant                    |   |
| SignalTap II Logic Analyzer         | © Compile test bench: synchronous_4bit_counter_to                         |
| PowerPlay Power Analyzer Settings   | Use script to set up simulation:  |
| SSN Analyzer                        | O Script to compile test <u>b</u> ench:                                   |
|                                     | More Nativel ink Settings   |
|                                     | <u>1000</u>   |
|                                     |   |
|                                     |   |
|                                     |   |
|                                     | We Buy Software OK Cancel Apply Help                                      |

| Vew Test Bench Settings   | ×                  |  |  |  |
|---|--------------------|--|--|--|
| Create new test bench settings.                                   |                    |  |  |  |
| Iest bench name: counter_4bit_tb                                  |                    |  |  |  |
| Top level <u>m</u> odule in test bench: counter_4bit_tb           |                    |  |  |  |
| Use test bench to perform VHDL timing simulation                  |                    |  |  |  |
| Design instance name in test bench: NA                            |                    |  |  |  |
| Simulation period   |                    |  |  |  |
| $\bigcirc$ Run simulation until all <u>v</u> ector stimuli are us | sed                |  |  |  |
| ● End simulation at: 700 ns ▼                                     |                    |  |  |  |
| Test bench and simulation files                                   |                    |  |  |  |
| Eile name:  | <u>A</u> dd        |  |  |  |
| File Name Library HDL Vers  | ion <u>R</u> emove |  |  |  |
| counter Default   | Цр                 |  |  |  |
|   | Down               |  |  |  |
|   | Properties         |  |  |  |
| ОК  | Cancel Help        |  |  |  |

no .vhdl extension

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- Example: Counter 4 bit
  - Run the simulation
    - Tools → Run Simulation Tool → RTL Simulation



Signal names visible

Verify the waveforms

Full simulation cycle plus restart visible

Note: ModelSim automatically zooms to the end of the simulation rt-click, view full, in the simulation window