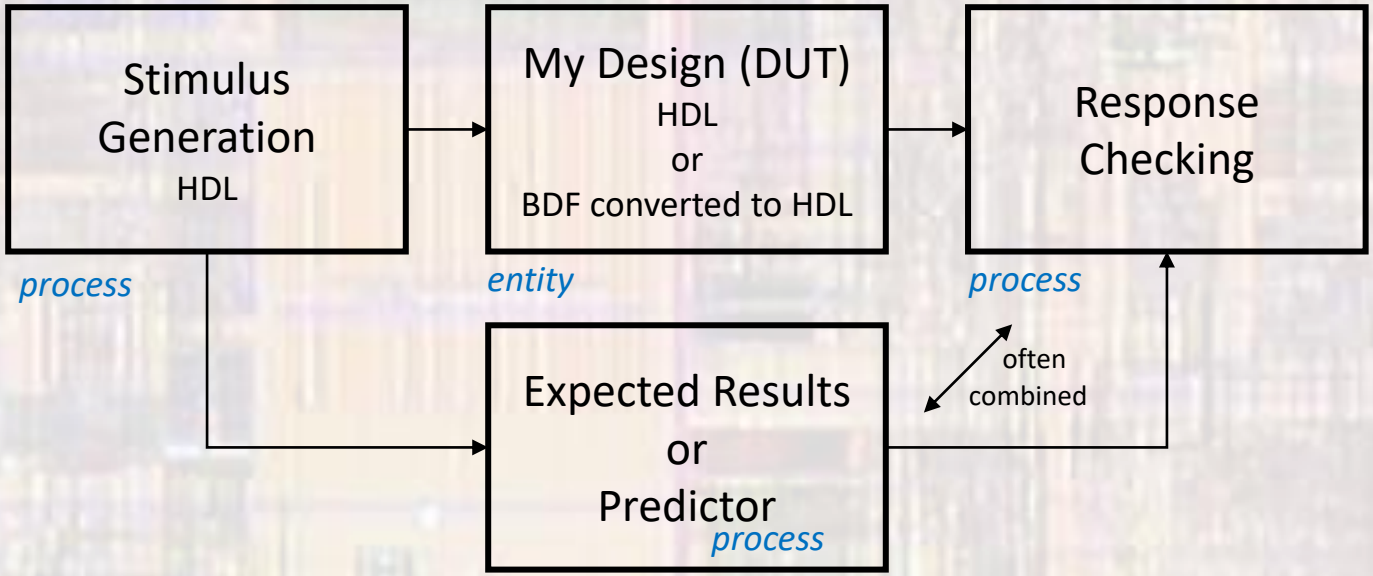
ModelSim Testbench
(HDL)

Common - last updated 3/9/20

ModelSim Testbench (HDL)

- Test Bench Concept



ModelSim Testbench (HDL)

- Example: Counter – 4bit
  - Create 4-b counter HDL

```
---Project Header---
--
-- counter_4bit.vhdl
-- Created: 2/23/18
-- By: johnsontimoj
-- For: CE1911
--

---Project Overview---
--
-- This project creates a binary counter
-- for the modelsim hdl example
--
--

--- Project Details ---
--
-- Inputs: rstb, clock
-- outputs: b0, b1, b2, b3
--
--

-- Library inclusion
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity counter_4bit is
   port( i_rstb:   in    std_logic;
         i_clk:    in    std_logic;

         o_cnt:    out   std_logic_vector(3 downto 0)
   );
end entity;
```

```
architecture behavioral of counter_4bit is
   --
   -- Internal Signals
   --
   signal cnt_sig:   unsigned(3 downto 0);

   begin
      --
      --  Update Section
      --
      process(i_clk, i_rstb)
      begin
         if (i_rstb ='0') then
            cnt_sig <= (others => '0');-- reset
         elsif (rising_edge(i_clk)) then
            cnt_sig <= (cnt_sig + 1);  -- count up
         end if;
      end process;

      --
      -- Output Section
      --
      o_cnt <= std_logic_vector(cnt_sig);

end architecture;
```

ModelSim Testbench (HDL)

- Example: Counter – 4bit
  - Create a test bench

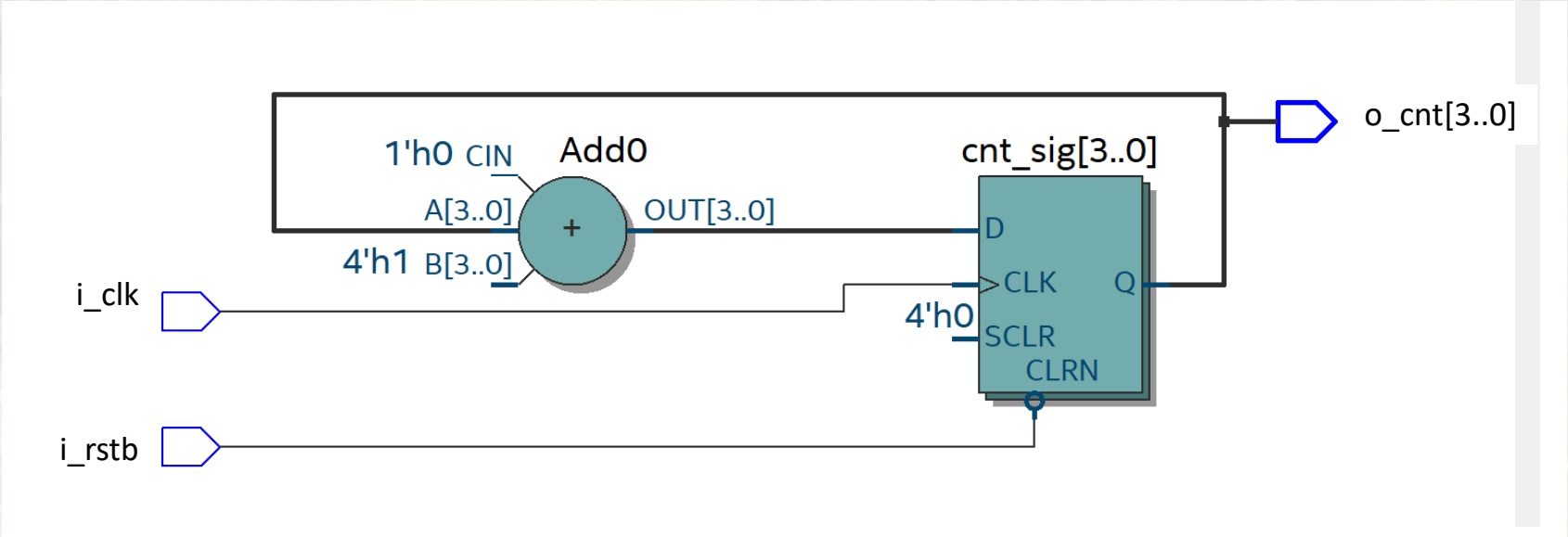
```
--------------------------------
--
-- counter_4bit_tb.vhdl
--
-- created: 1/26/18
-- by: johnsontimoj
-- rev: 0
--
-- testbench for 4 bit counter
-- of counter_4bit.vhdl
--
-- brute force implementation
--
--------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity counter_4bit_tb is
   -- no entry - testbench
end entity;
```

```
architecture testbench of counter_4bit_tb is
 signal   CLK:  std_logic;
 signal   RSTB: std_logic;

 signal   CNT:  std_logic_vector(3 downto 0);

 constant PER:  time  := 20 ns;

 ---------------------------------
 -- Component prototype
 ---------------------------------
 COMPONENT counter_4bit
    PORT
    (
       i_rstb      :   IN STD_LOGIC;
       i_clk       :   IN STD_LOGIC;
       o_cnt       :   OUT STD_LOGIC_vector(3 downto 0)
    );
 END COMPONENT;
 -----------------------------------
```

```
  begin

  -----------------------------------
  -- Device under test (DUT)
  -----------------------------------
  DUT: counter_4bit
     port map(
               i_rstb    => RSTB,
               i_clk     => CLK,
               o_cnt     => CNT
               );


  -----------------------------------
  -- Test processes
  -----------------------------------

  -- Clock process
  clock: process    -- no sens list allowed
     begin
        CLK <= '0';
        wait for PER/2;
        infinite: loop
           CLK <= not CLK; wait for PER/2;
        end loop;
  end process;

  -- Reset process
  reset: process    -- no sens list allowed
     begin
        RSTB <= '0'; wait for 2*PER;
        RSTB <= '1'; wait;
  end process reset;

  -- Run Process
  -- No run process for this design

  -------------------------------------------
  -- End test processes
  -------------------------------------------

end architecture;
```

ModelSim Testbench (HDL)

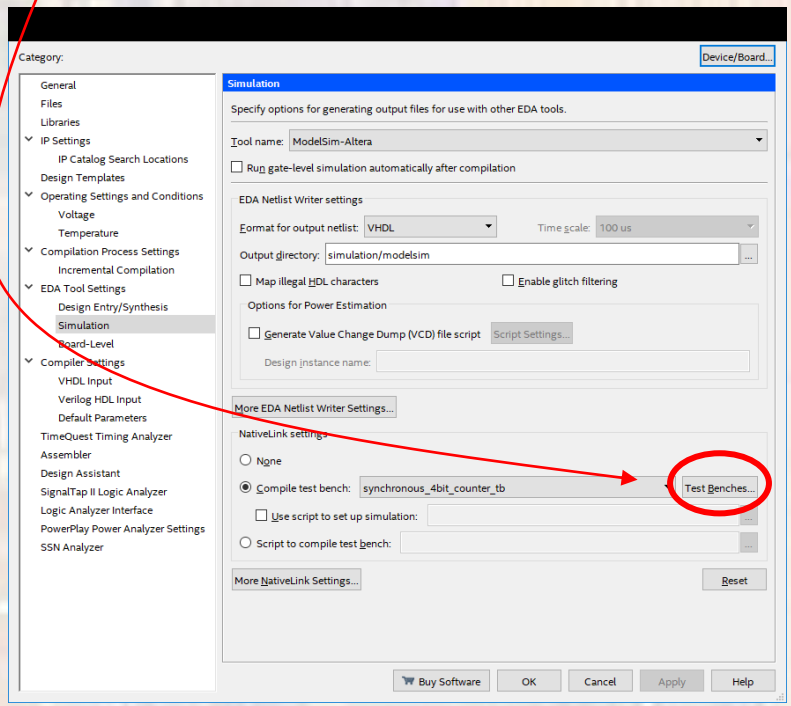
- Example: Counter – 4 bit
  - Elaborate the design (create RTL)
    - Note: leave the main design as the top level block
    - Processing → Start → Start Analysis and Elaboration
  - Check the RTL
    - Tools → Netlist Viewers → RTL Viewer

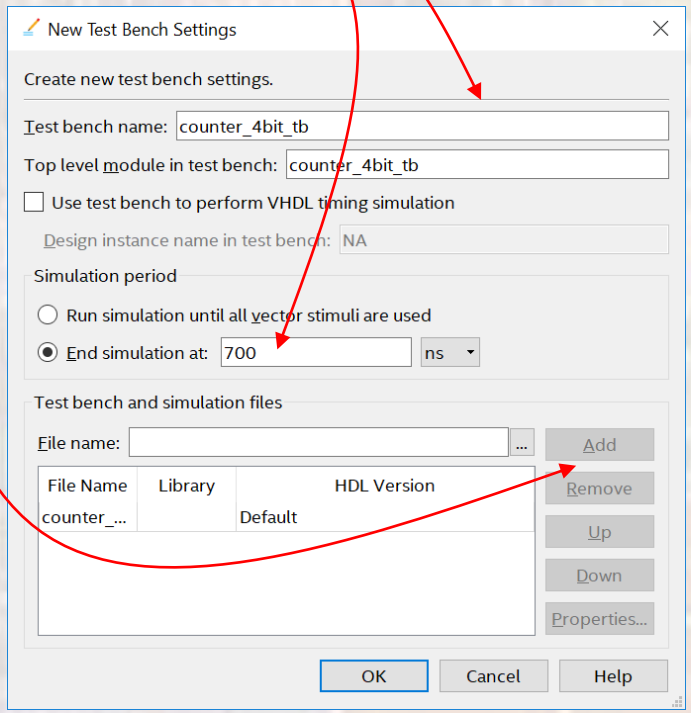


ModelSim Testbench (HDL)

- Example: Counter – 4 bit
  - Setup the test bench
    - Assignments → Settings → EDA Tool Settings → Simulation → Test Benches :
      : enter the test bench file
      : select the end simulation time
      : select File name … and select the test bench file

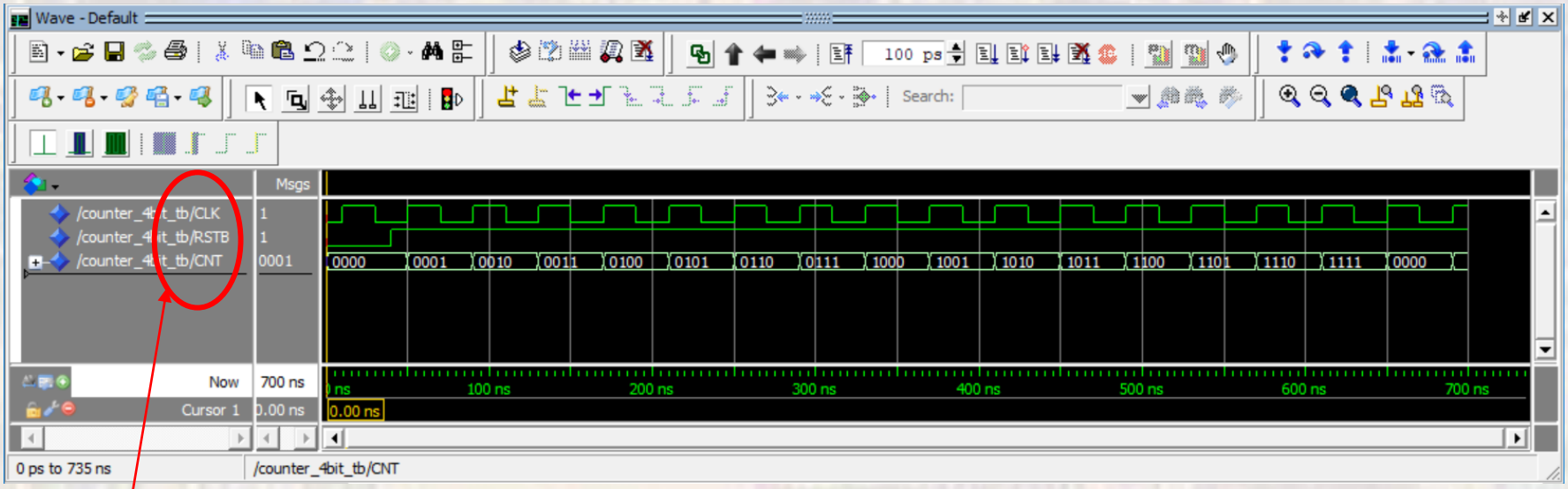
no .vhdl extension





ModelSim Testbench (HDL)

- Example: Counter – 4 bit
  - Run the simulation
    - Tools → Run Simulation Tool → RTL Simulation



Signal names visible

- Verify the waveforms

Full simulation cycle plus restart visible

Note: ModelSim automatically zooms to the end of the simulation
rt-click, view full, in the simulation window