

- Quartus Prime Project Setup
 - Before creating your first Quartus project:
 - Install the Quartus software see "Quartus Software Setup"
 - Projects are created for a top level design
 - Create a project directory to keep all of your projects organized
 - Eg. .../HDL/Quartus_Projects
 - Your project folder should be placed somewhere in your personal folder path – Not in the Quartus installation directory

- Quartus Prime Project Setup
 - Quartus uses directories to store projects in
 - Create a separate directory for each project
 - Eg. .../HDL/Quartus_Projects/MyFirstDE10Project

No spaces in the directory path

It's best to not use any special characters in the project folder name

- Quartus Prime Project Setup
 - Start the Quartus software
 - Under File select New Project Wizard ...

	5	S Quartus Prime Lite Edition									
	File	Edit View	Project	Assignments	Processing	Tools	Window Help				
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		Close		Ctrl+F4	C	DLLA	BORATE. DESIGN. IN				
	A	New Project Wi	zard	>			iartus' Prime				
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	Ξ	Save		Ctrl+S							
		Save As									
2	с ^{ра}	Save All		Ctrl+Shift	t+S		Q				
		File Properties.									
	47 1			Ctrl+Shift	t+S		Q				

- Quartus Prime Project Setup
 - Select Next

🕥 New Project Wizard

Introduction

The New Project Wizard helps you create a new project and preliminary project settings, including the following:

- Project name and directory
- Name of the top-level design entity
- Project files and libraries
- Target device family and device
- EDA tool settings

You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.

Don't show me this introduction again

Common

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Next >

Finish

Cancel

Help

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- Quartus Prime Project Setup
 - Select your project directory
 - •/Name your project
 - Your project name and top level entity name should be

the same

Click Next

New Project Wizard
 Directory, Name, Top-Level Entity
 What is the working directory for this project?
 C:/ ••• /Projects/MyFirstDE10Project
 What is the name of this project?
 MyFirstCounter
 What is the name of the top-level design entity for this project? This name is case so design file.
 MyFirstCounter
 Lyse Existing Project Settings...

- Quartus Prime Project Setup
 - Select Empty project
 - Click Next

New Project Wizard
Project Type
Select the type of project to create.
<u>E</u> mpty project
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.

Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the <u>Design Store</u>.

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- Quartus Prime Project Setup
 - We will not add any files right now
 - Click Next

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Add Files

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.

Note: you can always add design files to the project later.

•								×	
~								**	Add
File Name	Type L	.ibrary	Design Entry/Synthesis Tool	HDL Versio	on				<u>R</u> em
									U
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- Quartus Prime Project Setup
 - Select Max 10 (DA/DF/DC/SA/SC) under Family
 - Select Max 10 DA under Device
 - Select 10M50DAF484C7G under Available devices
 - Click Next

Device Board								
	device you want to tar onal device support wi	-	•	and on the Tool	s menu.			
o determine the ver	sion of the Quartus Pri	me softwar	e in which your ta	rget device is s	upported, refer to th	ne <u>Device Support List</u> webpag		
Device family				Show in 'Availat	ole devices' list			
Eamily: MAX 10 (I	DA/DF/DC/SA/SC		-	Pac <u>k</u> age:	Any	•		
Dev <u>i</u> ce: MAX 10	DA		•	Pin <u>c</u> ount:	Any	•		
Target device				Core sp <u>e</u> ed grad	de: Any			
O <u>A</u> uto device sele	ected by the Fitter			Name filter:				
Specific devices Other: n/a	selected in 'Available d	evices' list		☑ S <u>h</u> ow advanced devices				
vailable devices:								
Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9		
10M50DAF484C7G	1.2V	49760	360	360	1677312	288		
<						>		

Quartus Prime – Project Setup

New Project Wizard

- Under simulation select ModelSim-Altera and VHDL
- Click Next

EDA Tool Settir	ngs		
	tools used with the Quar	tus Prime software	e to develop your project.
EDA tools:			
Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synth	<none></none>	<none></none>	abla Run this tool automatically to synthesize the current design
Simulation 🤇	ModelSim-Altera	VHDL	Run gate-level simulation automatically after compilation
Board-Level	Timing	<none></none>	•
	Symbol	<none></none>	•
	Signal Integrity	<none></none>	•
	Boundary Scan	<none></none>	~

< Back

Next >

<u>F</u>inish

Cancel

Note: ModelSim-Altera not ModelSim

Help

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- Quartus Prime Project Setup
 - You will get a summary window
 - Click Finish

S New Project Wizard

Summary

When you click Finish, the project will be created with the following settings:

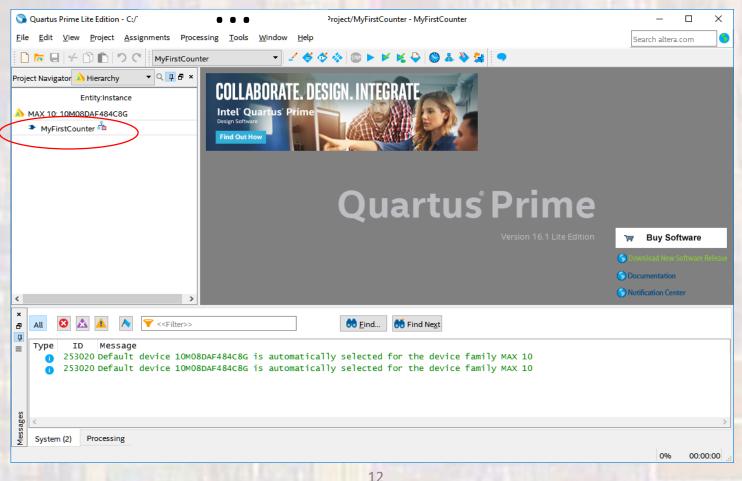
then yes each much are project and be created and are reasoning security.								
Project	: directory:	C:/Tim/GDrive/MSOE/18_Q1_EE3921/Projects/MyFirstDE10Project						
Project name:		MyFirstCounter						
Top-le	vel design entity:	MyFirstCounter						
Numb	er of files added:	0						
Numb	er of user libraries added:	0						
Device	assignments:							
	Design template:	n/a						
	Family name:	MAX 10 (DA/DF/DC/SA/SC)						
	Device:	10M50DAF484C7G						
	Board:	n/a						
EDA to	ols:							
	Design entry/synthesis:	<none> (<none>)</none></none>						
	Simulation:	ModelSim-Altera (Verilog HDL)						
	Timing analysis:	0						
Operat	ing conditions:							
	Core voltage:	1.2V						
	Junction temperature range:	0-85 °C						
		< <u>Back</u> Next > <u>F</u> inish Cancel <u>H</u> elp						

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Quartus Prime – Project Setup

Common

 Your project will now appear in the Project Navigator window



- Quartus Prime Project Setup
 - We will be using the 2008 version of VHDL
 - Assignments -> Settings -> Compiler Settings -> VHDL Input
 - Select VHDL 2008

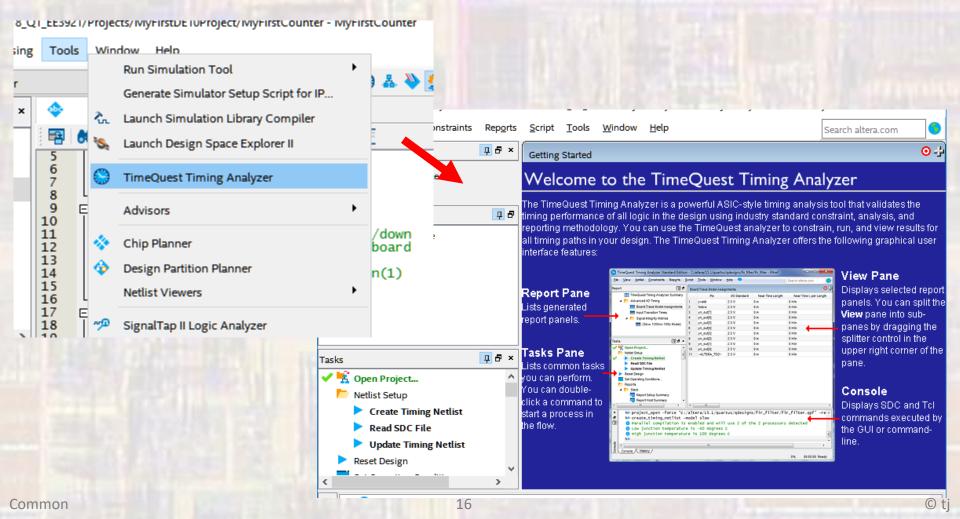
Category:	Device/Board
General	VHDL Input
Files Libraries	Options for directly compiling or simulating VHDL input files. (Click on the EDA Tool Settings category to enter options for VHDL files generated by other EDA tools.)
Libraries Libraries IP Settings IP Catalog Search Locations Design Templates Operating Settings and Conditions Voltage Temperature Compilation Process Settings Incremental Compilation EDA Tool Settings Design Entry/Synthesis Simulation Board-Level Compiler Settings VHDL Input Verilog HDL Input Default Parameters TimeQuest Timing Analyzer Assembler Design Assistant Signal Tap Logic Analyzer Logic Analyzer Interface Power Analyzer Settings SSN Analyzer	
	Buy Software OK Cancel Apply Help

- Quartus Prime Project Setup
 - If you plan to run the project on the DE10 and
 - you want to use the assigned pin names (recommended)
 - you need to import the DE10_Lite.qsf file from the web page
 - right click the link and save link as (DE10_Lite.qsf, QSF file type) in the project directory
 - Assignments -> Import Assignments
 - Point to your downloaded DE10_Lite.qsf file

S Import Assignments	×
Specify the source and categories of assignments to import.	
Eile name: C://DE10_Lite.qsf	Categories
Copy existing assignments into MyFirstCounter.qsf.bak before im	Advanced
OK Cancel	Help

- Quartus Prime Project Setup
 - Proper placement and routing requires that the design meets a set of timing requirements
 - A very basic set of timing requirements is available in the file Basic_SDC.sdc on the web site
 - You will use this as a starting point for each project you create

- Quartus Prime Project Setup
 - Select Tools -> TimeQuest Timing Analyzer



- Quartus Prime Project Setup
 - Select File -> New SDC File
 - Copy and paste the contents of Basic_SDC.sdc into the file

	File	View Netlist	Constraints	Reports	Script	Tools	Windc	A T		
		New SDC File		₽ ×	Getting	Started	_		xt Editor - C:/Tim/GDrive/MSOE/18_Q1_EE3921/Projects/MyFirstDE10Project/MyFirstCounter - MyFirstCounter - [M — 🗆 🗙	•
1	~	Open Close	Ctrl+O		Welc		to t	48 49 50	60 (7) [書 律 四 四 10 ▲ ② 號 亜 # Set Clock Groups #***************	^
		Page Setup Print Preview Print	Ctrl+P	<u> </u>	The Time timing per reporting all timing interface f	formanc methodo paths in	e of all blogy, Y your de	50 51 52 53 54 55 56 57 58 59 60	#*************************************	
		SDC Files	•		Report	Pane	Director (le Xe Reput	61 62 63 64 65 66 67 68	#*************************************	
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									Ln 85 Col 64 Synopsys Design Constraints File 0% 00:00:00	

- Quartus Prime Project Setup
 - Select File -> Save As
 - Name the file the same as your project name
 - It should default to your output files directory
 - Save and close the TimeQuest window

Save As			×
← → • ↑ 📘	« MyFirstDE10Project → output_files v č) Search output_fi	les ,0
Organize 🔻 Ne	w folder		::: • ?
💻 This PC	^ Name	Date modified	Туре
Desktop	MyFirstCounter.sdc	8/31/2017 1:33 PM	SDC File
Documents			
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Yideos			
骗 TI10716000F ((C:)		
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File <u>n</u> ame:	MyFirstCounter.sdc		~
Save as <u>t</u> ype:	Synopsys Design Constraints Files (*.sdc)		~
∧ Hide Folders	Add file to current project	<u>S</u> ave	Cancel .::

- Quartus Prime Project Setup
 - Configure the tools for the DE10_Lite board Assignments -> Device -> Device and Pin Options -> Configuration -> Configuration Mode and select

single uncompressed Image with Memory Initialization

Device and Pin Options - LAB3				0
tegory:				
General Configuration Programming Files Unused Pins Dual-Purpose Pins Capacitive Loading Board Trace Model I/O Timing Voltage Pin Placement Error Detection CRC CvP Settings Partial Reconfiguration	Configuration scheme: Configuration mode: Configuration device Use configuration Configuration device	Single Compressed Image (5888Kbits UFM) Single Compressed Image with Memory Initial Single Uncompressed Image (3584Kbits UFM) Single Uncompressed Image with Memory Init	tialization (512Kbits UFM) ization (512Kbits UFM)	•
	Generate compress	ed bitstreams	Comparation Pin Options	

Quartus Prime – Project Setup

• Your project is ready to use