Questa Simulation Tips

Common - last updated 9/14/26

Questa Tips

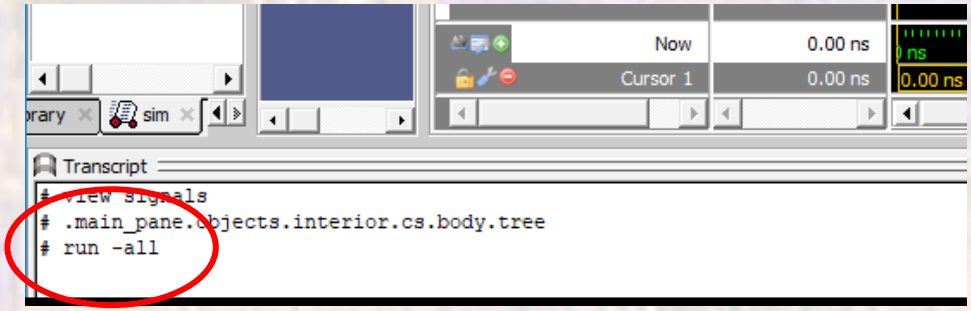
- Simulation “tips”

  - Your simulation says it’s running but it never stops P3
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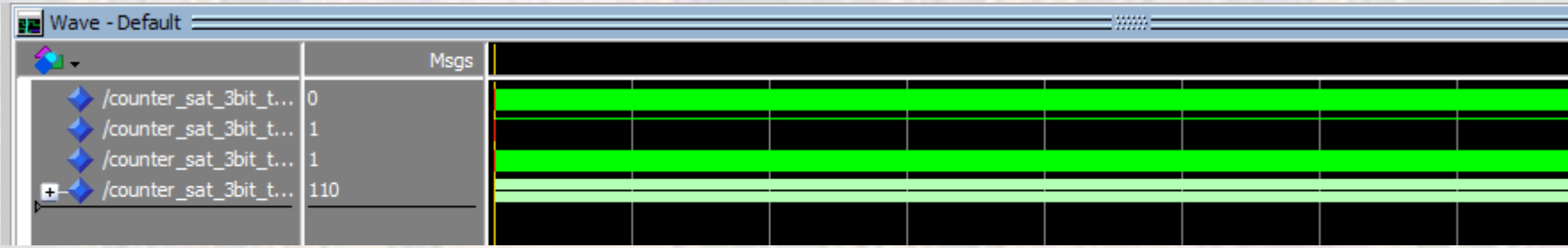
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Questa Tips

- Simulation Run
  - Your simulation says it's running but it never stops



  - OR
  - You stopped your simulation and the results just look like a solid line

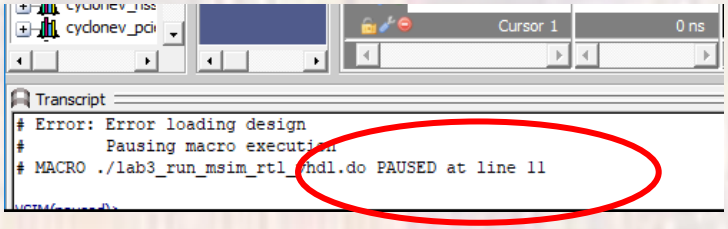


  - Issue: You failed to set the simulation time when creating the test bench in assignments→ settings→ simulation

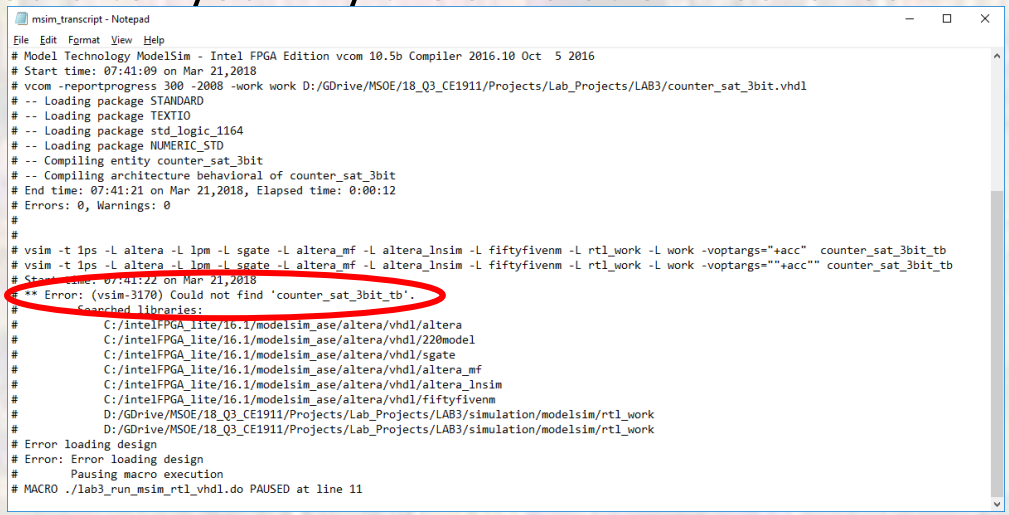
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Questa Tips

- Simulation Run
  - Your simulation fails for some reason



  - Go to your project directory/simulation/questa and open the file msim_transcript in notepad
    - It should tell you why the simulation has failed



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Questa Tips

- Extending the time of a simulation
  - You setup your testbench and ran the simulation (it took a long time to run)
  - You need to run the simulation for a little longer (or a lot)
  - You could stop the simulation, modify the testbench simulation time parameter and restart

  OR

  - In ModelSim

    Simulate -> Runtime Options… -> Default Run

    set the default run to the desired simulation extension, e.g. 1000 ns

    Simulate -> Run -> Run 100

    hitting Run 100 will run the simulation again, and again, and … each time extending the desired amount of time

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Questa Tips

- Adding internal signals to the simulation
  - You setup your testbench and ran the simulation
  - Something is not working and you need to see an internal signal to figure out what is happening
  - You could stop the simulation, add I/Os to the design to see the internal signals, elaborate and re-run the simulation

OR

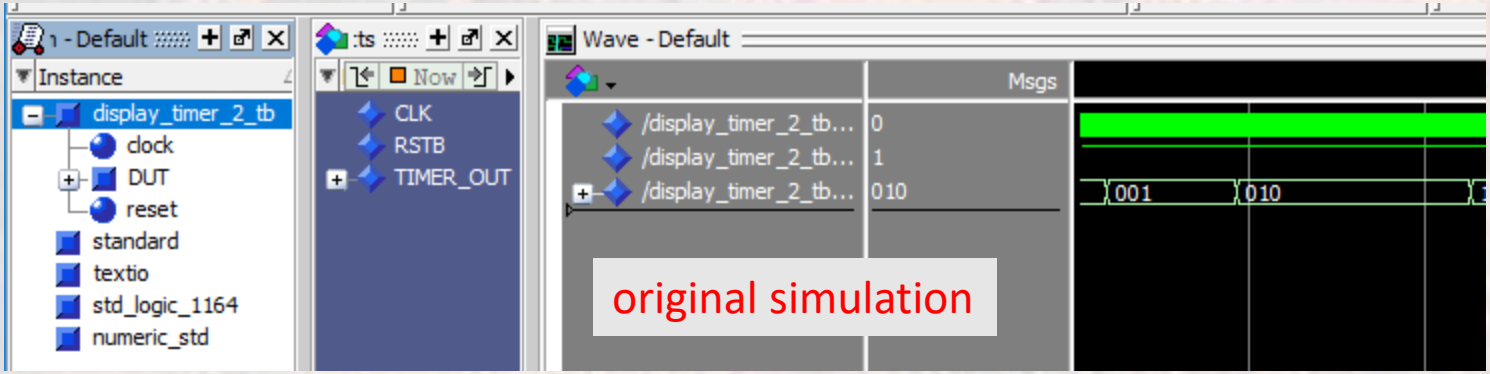
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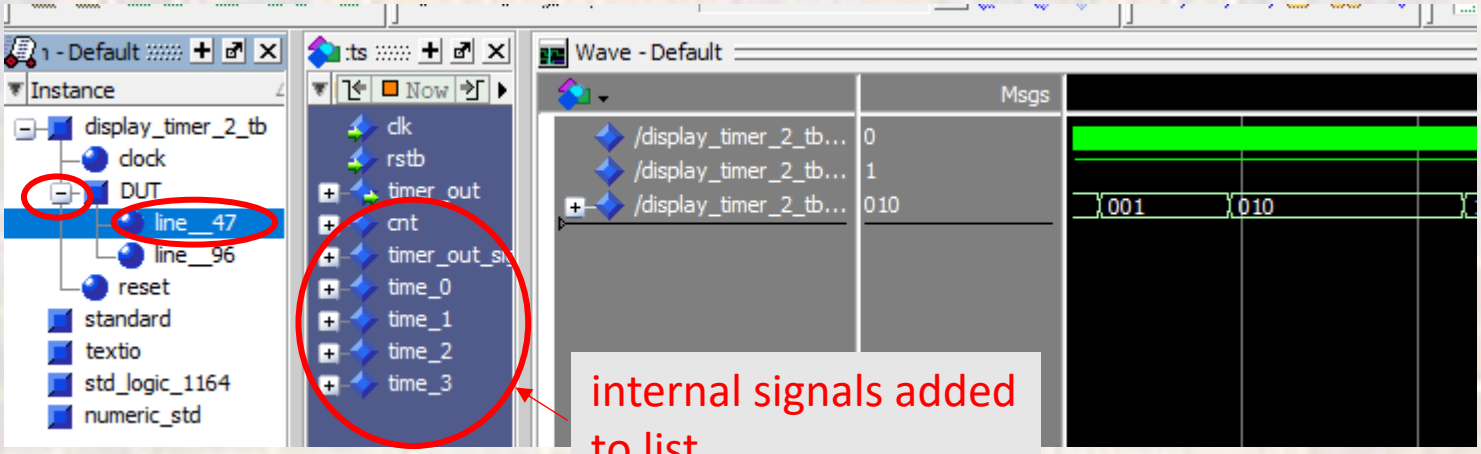
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Questa Tips

- Adding internal signals to the simulation



expand the DUT and select one of the lines

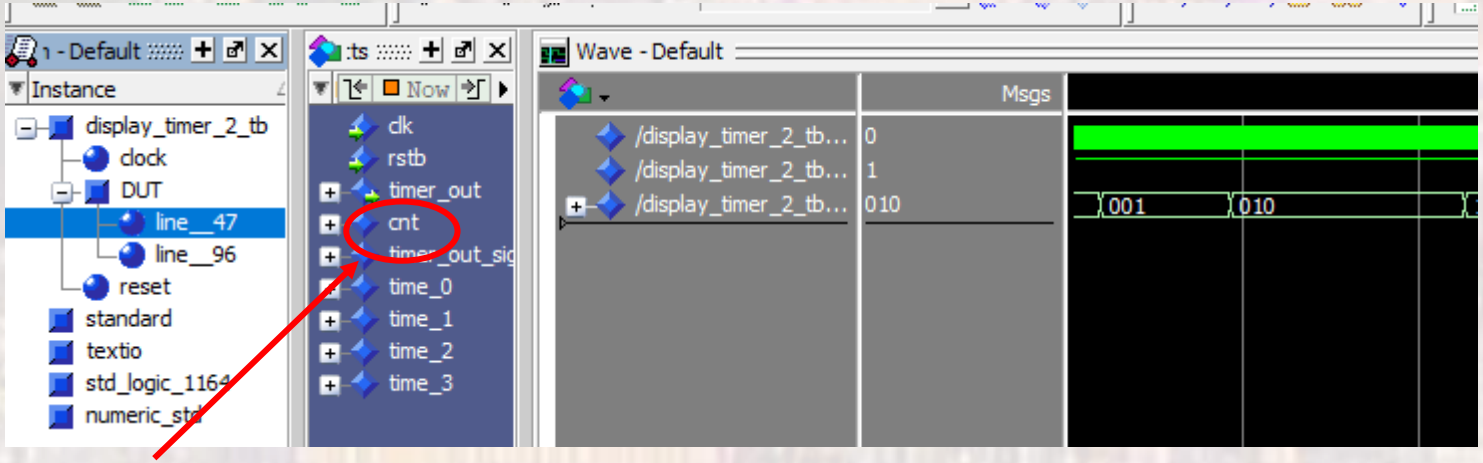


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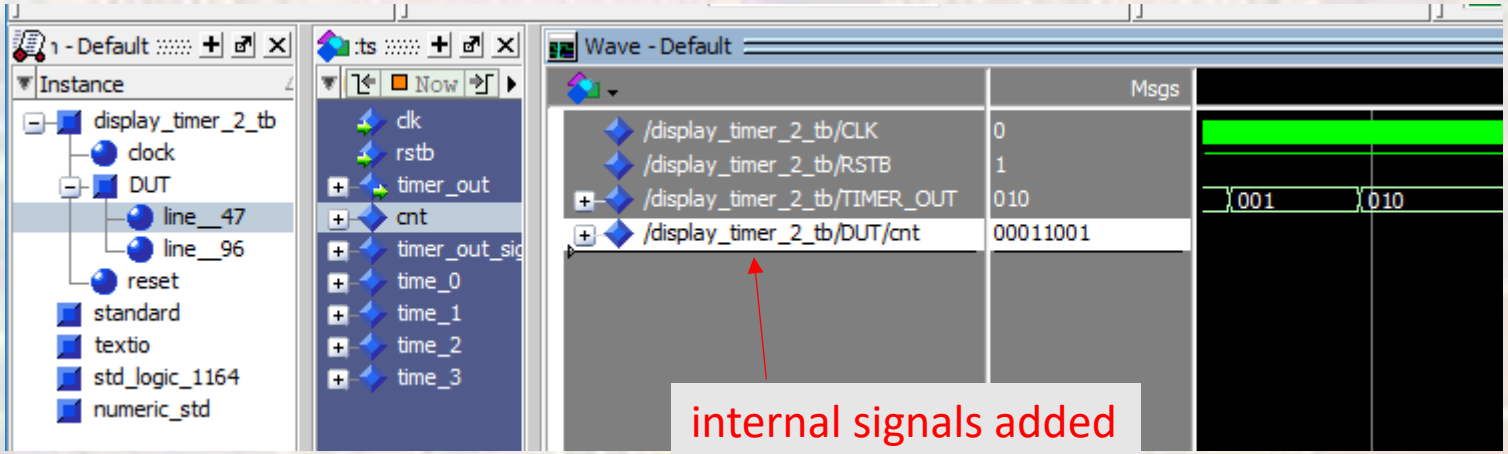
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Questa Tips

- Adding internal signals to the simulation



right click on the signal you want to add and select Add Wave



Cont'd

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Questa Tips

- Adding internal signals to the simulation

  simulate -> restart

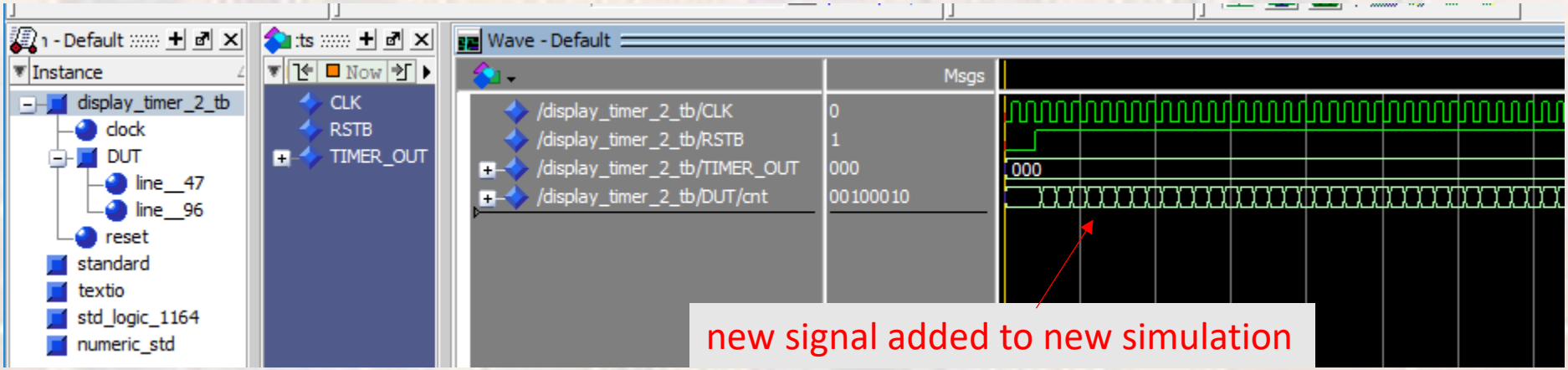
  click OK

  Simulate -> Runtime Options… -> Default Run

  set the default run to the desired simulation time, e.g. 3000 ns

  Simulate -> Run -> Run 100

  hitting Run 100 will run the simulation again with the new signal added



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Questa Tips

- Save your waveform format to reuse
  - Add any signals
  - Choose Radix, …

  File -> Save Format

  Will default to something like
  …/project/simulation/modelsim/wave.do
  you can make as many .do files as you wish

- To reload

  File -> Load -> Macro File

  Point to your desired .do files

  Note: you will get duplicates of your original signals

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Questa Tips

- Changing your VHDL file or testbench without restarting Questa
  - Make any changes to your testbench
    - No need to run Analyze and Elaborate
  - Make any changes to your VHDL
    - Be sure to rerun Analyze and Elaborate

  - In Questa (already open)

    Files -> Load -> Macro File

    select Project-name_run_msim_rtl_vhdl.do

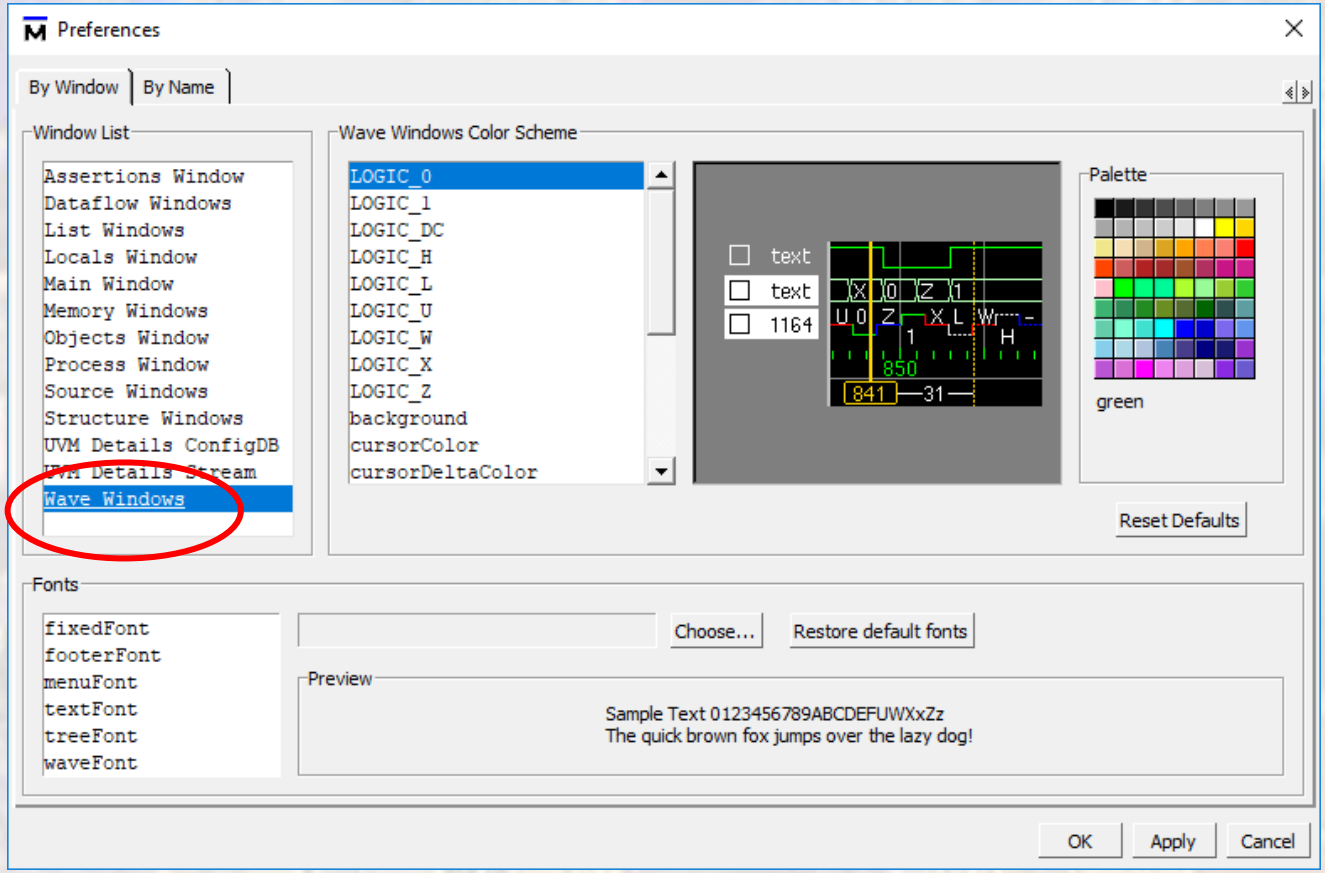
    - Your original simulation will rerun using the new files

    Note: You will have to reload any wave changes you made

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Questa Tips

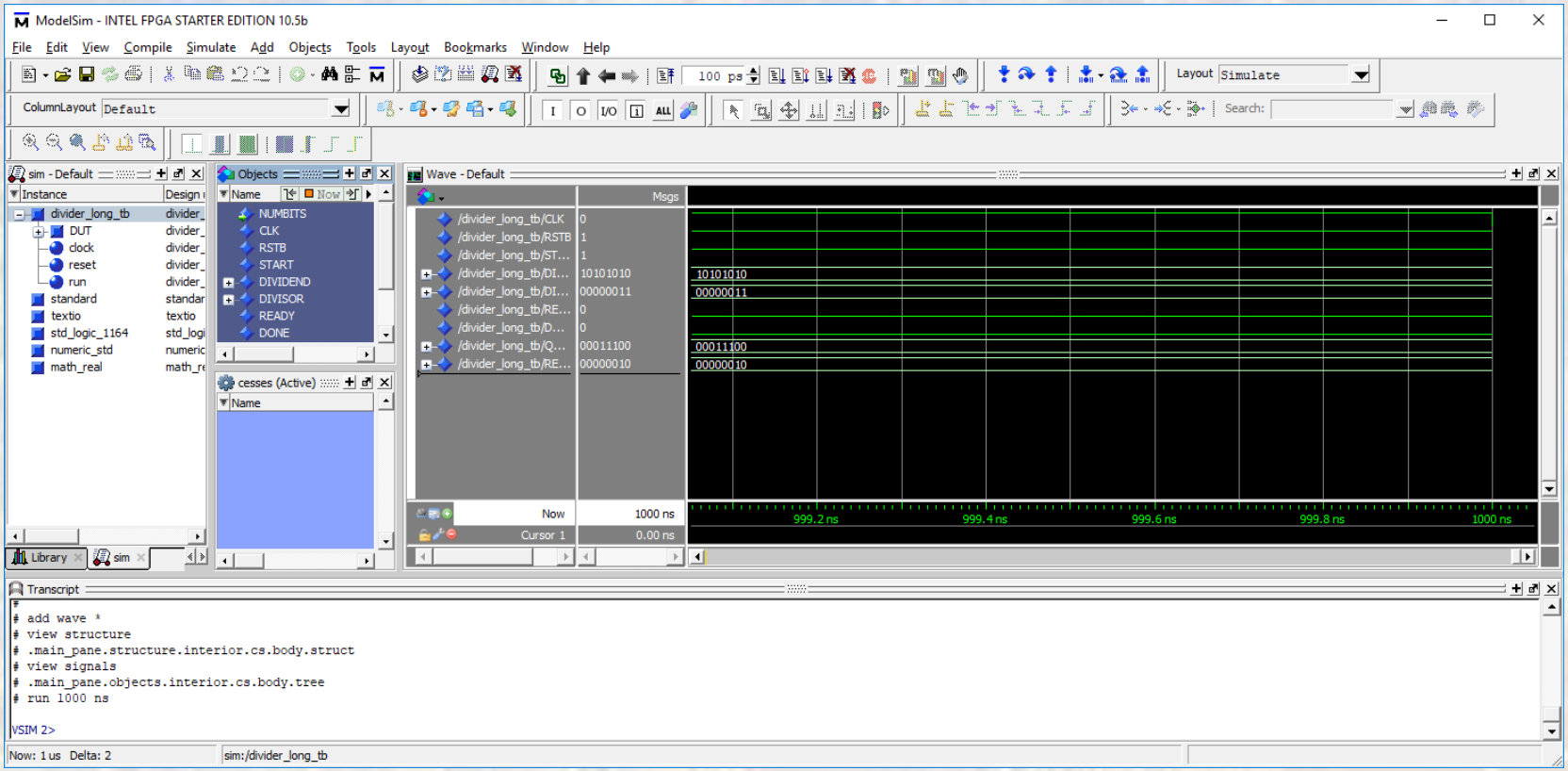
- Can I change the way waveforms look (colors)
  - Tools -> Edit Preferences -> Wave Windows



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Questa Tips

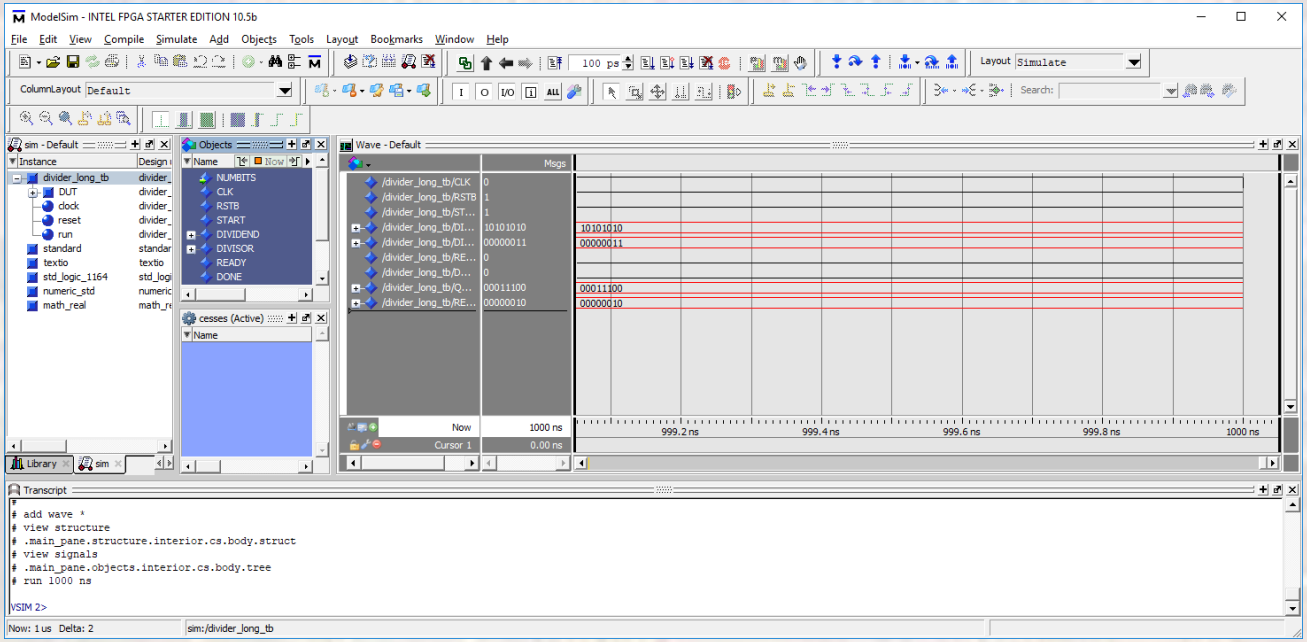
- Can I change the way waveforms look (colors)
  - Default Colors



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Questa Tips

- Can I change the way waveforms look (colors)
  - waveformBackground → white
    (scroll down in Wave windows color screen)
  - Logic0, Logic1, Text, Time → black
  - Vector → red



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