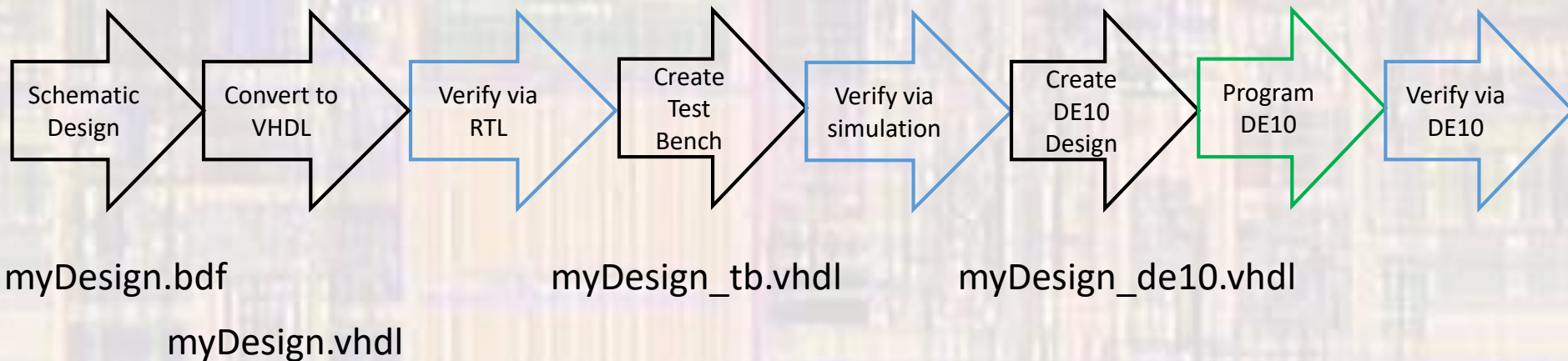


# Schematic Project Example

Common - last updated 2/11/19

# Schematic Project Example

- Project Flow

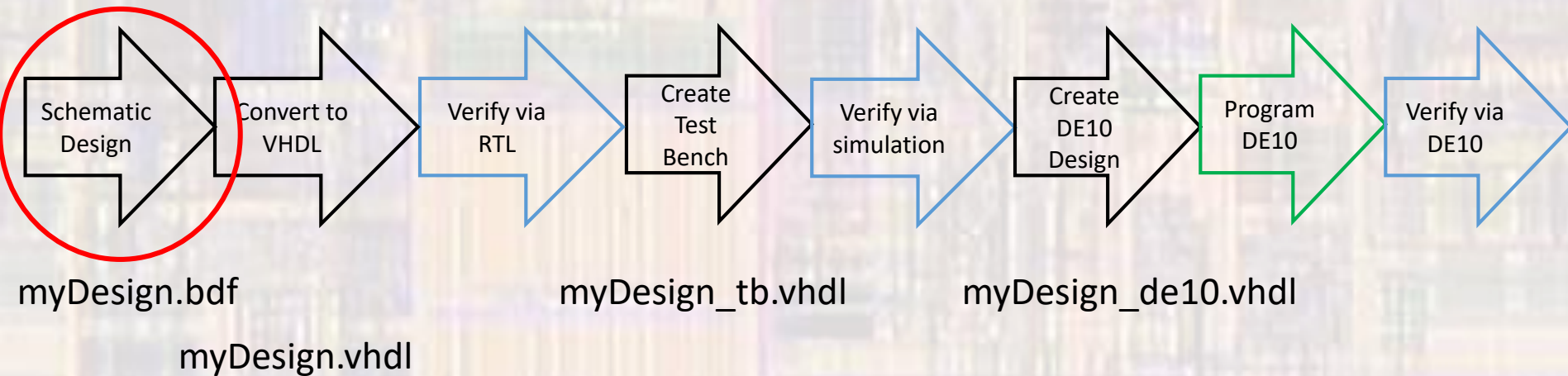


# Schematic Project Example

- Create a new Project
  - Select **File** -> **New Project Wizard**
    - ...
    - See project setup slides if necessary

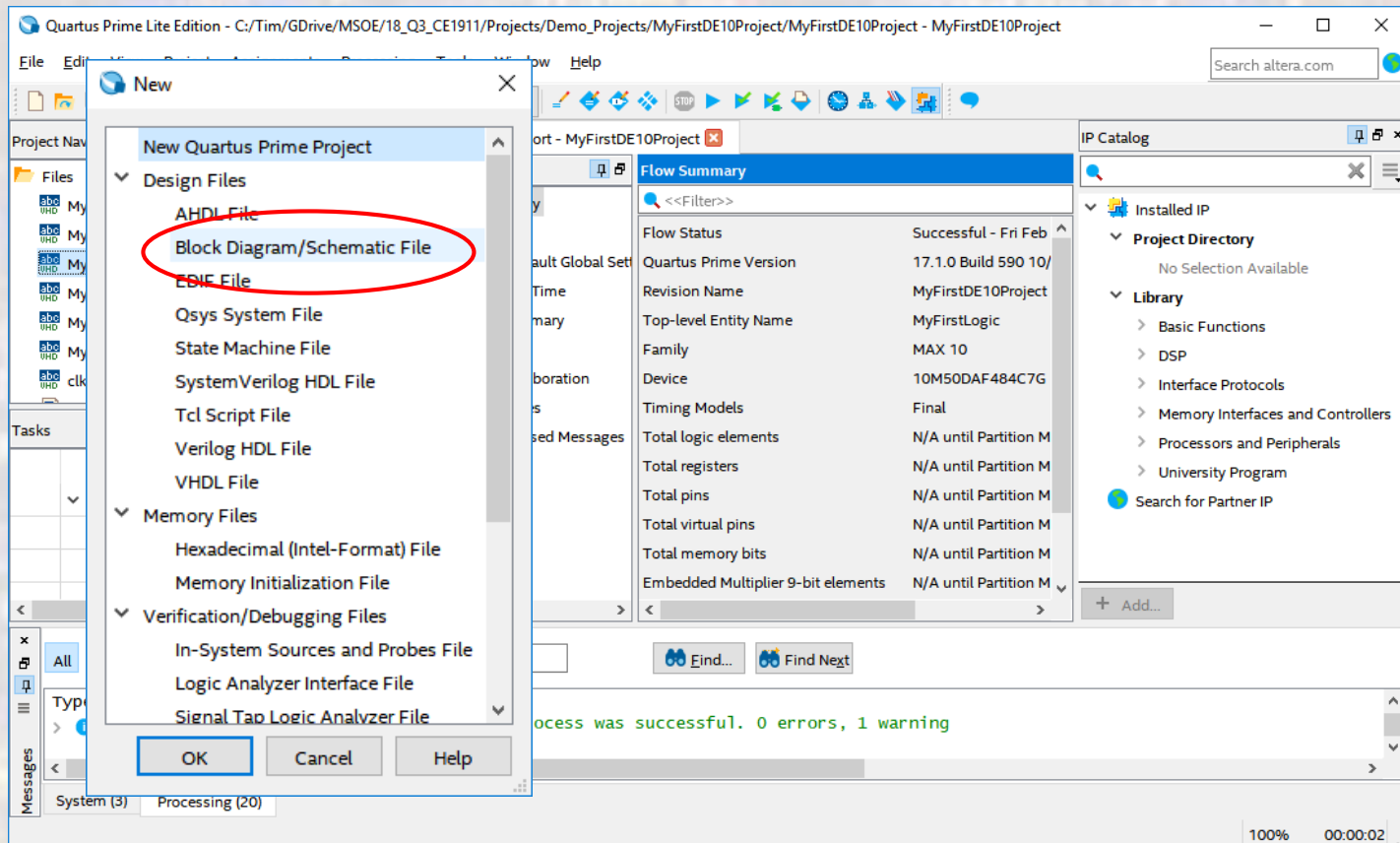
# Schematic Project Example

- Project Flow



# Schematic Project Example

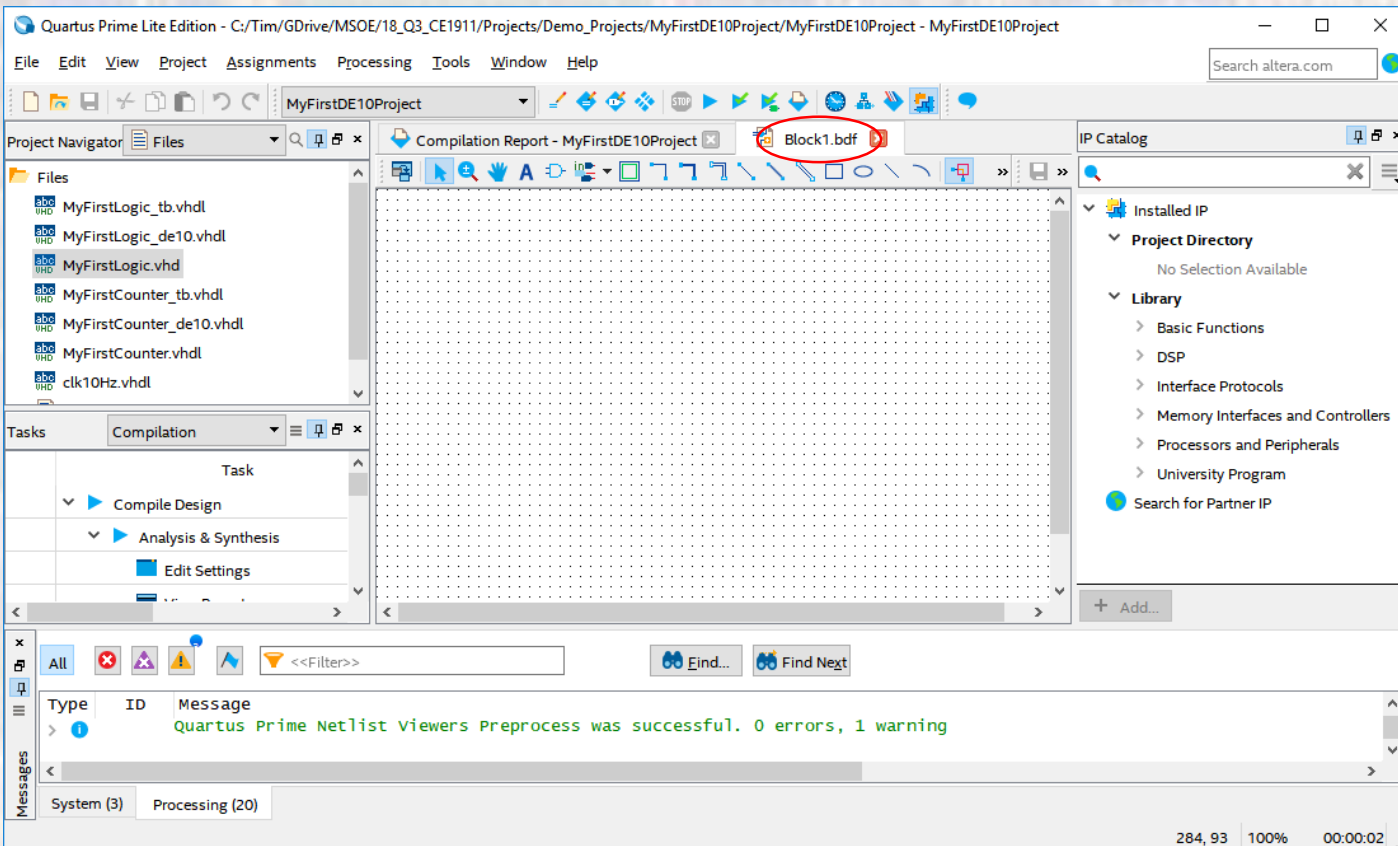
- Create a new BDF file
  - Select **File** -> **New** -> **Block Diagram/Schematic File**





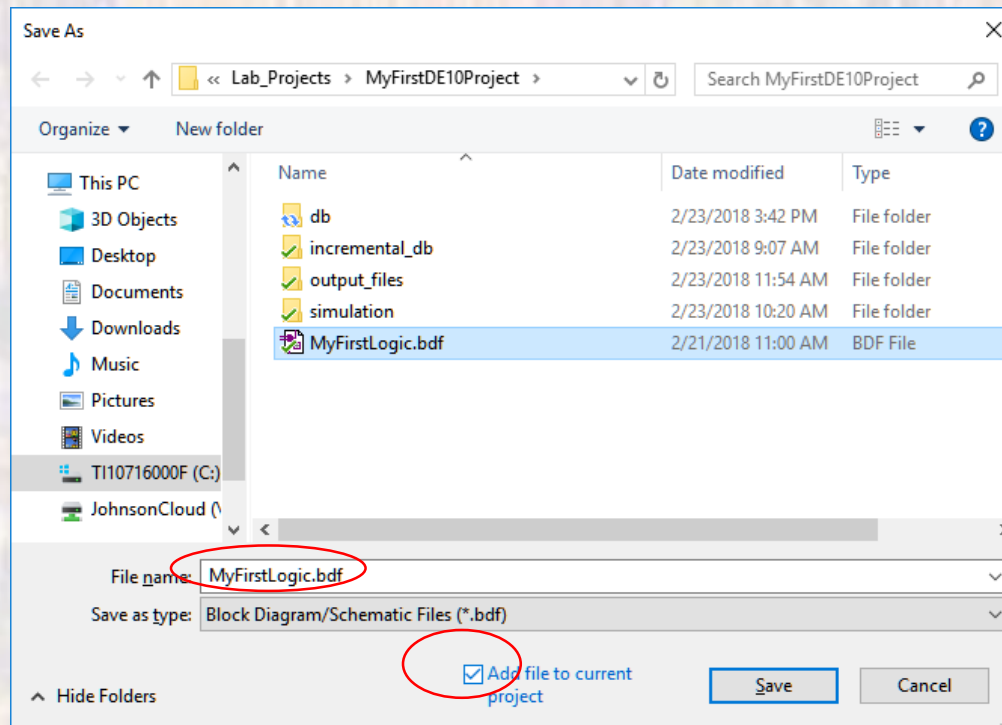
# Schematic Project Example

- Create a new BDF file
  - Note the default file name
  - We want this to be our top level entity so we must change the name



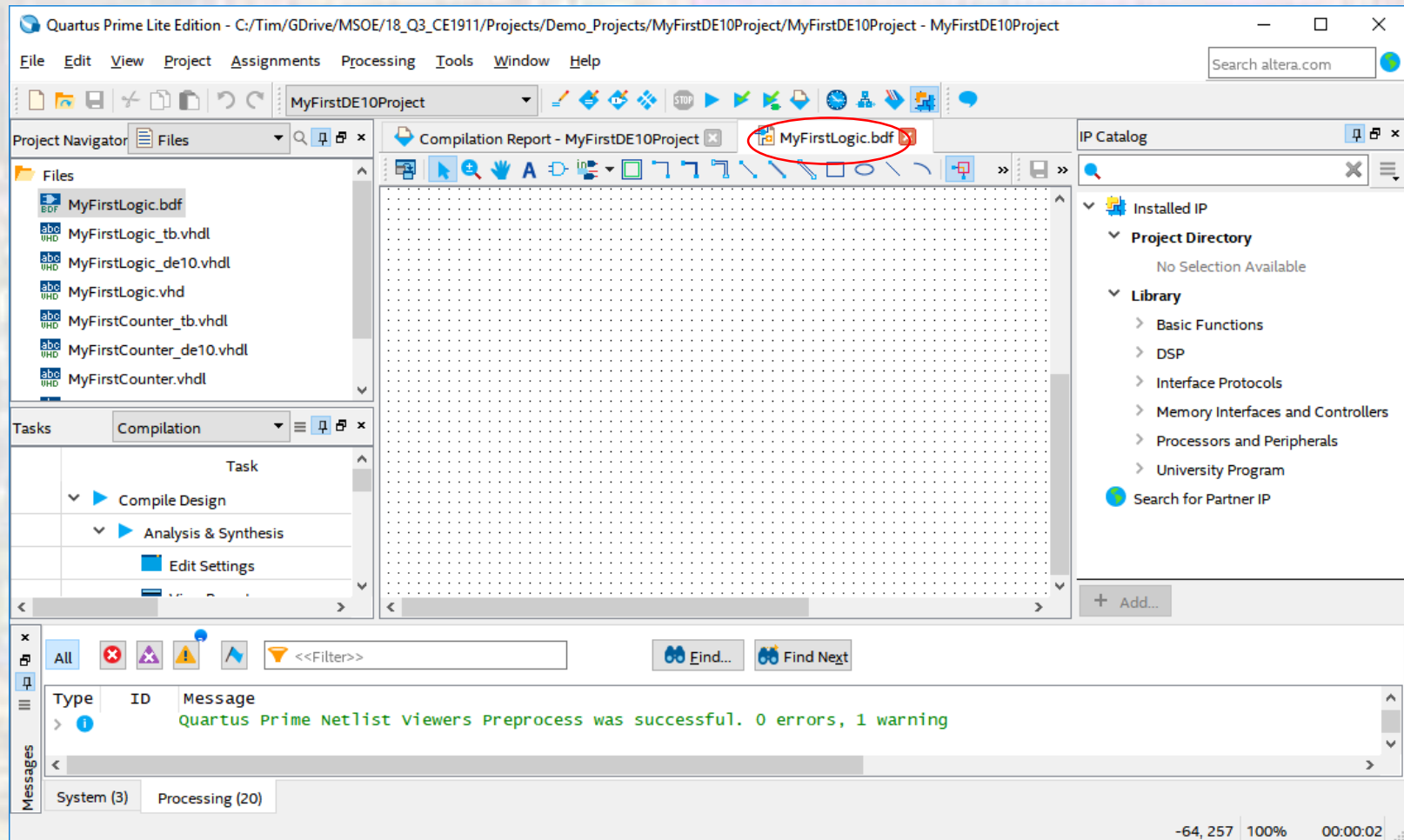
# Schematic Project Example

- Create a new BDF file
  - Select **File** -> **Save As**
  - Set the file name to the our desired value
  - Make sure “**Add file to current project**” is checked



# Schematic Project Example

- Create a new BDF file
  - Note the name change





# Schematic Project Example

- Create a new BDF file
  - Create your schematic

The screenshot displays the Quartus Prime Lite Edition interface for a project named "MyFirstDE10Project". The main window shows a schematic diagram of a logic circuit with two inputs, "inout1" and "inout2", and two outputs, "out1" and "out2". The circuit consists of several logic gates, including AND gates (labeled "AND12" through "AND17") and OR gates (labeled "OR12" through "OR17"). The gates are interconnected to perform a logical function. The interface includes a Project Navigator on the left showing the project files, a Tasks pane with "Compile Design" and "Analysis & Synthesis" options, and an IP Catalog on the right. The Messages pane at the bottom shows a successful compilation message: "Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning".

Quartus Prime Lite Edition - C:/Tim/GDrive/MSOE/18\_Q3\_CE1911/Projects/Demo\_Projects/MyFirstDE10Project/MyFirstDE10Project - MyFirstDE10Project

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

MyFirstDE10Project

Project Navigator Files

- MyFirstLogic.bdf
- MyFirstLogic\_tb.vhdl
- MyFirstLogic\_de10.vhdl
- MyFirstLogic.vhd
- MyFirstCounter\_tb.vhdl
- MyFirstCounter\_de10.vhdl
- MyFirstCounter.vhdl

Tasks Compilation

- Task
- Compile Design
- Analysis & Synthesis
- Edit Settings

Compilation Report - MyFirstDE10Project

MyFirstLogic.bdf

IP Catalog

- Installed IP
- Project Directory
  - No Selection Available
- Library
  - Basic Functions
  - DSP
  - Interface Protocols
  - Memory Interfaces and Controllers
  - Processors and Peripherals
  - University Program
- Search for Partner IP

Messages

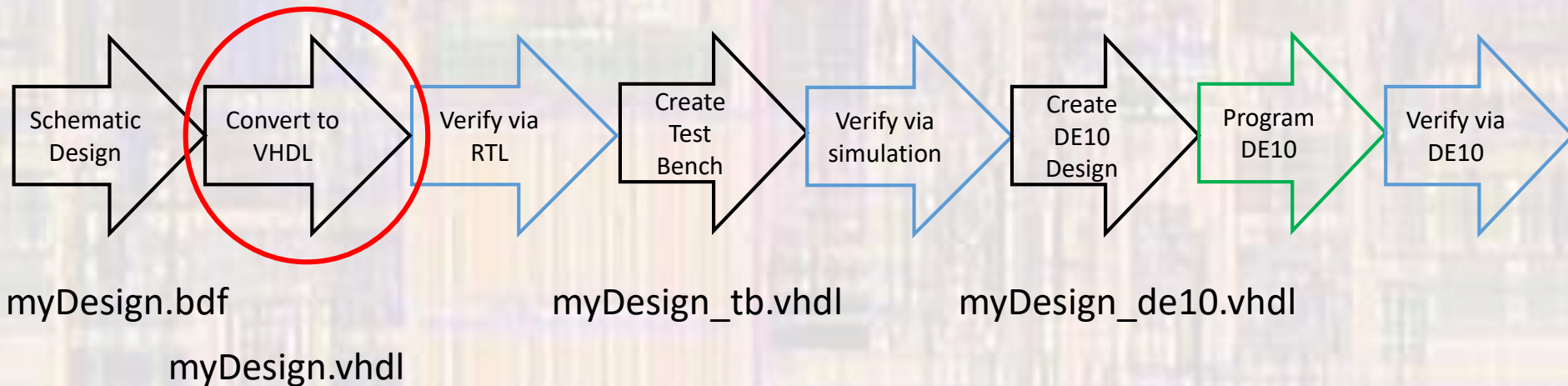
Type	ID	Message
Info		Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning

System (3) Processing (20)

-24, -41 100% 00:00:02

# Schematic Project Example

- Project Flow



# Schematic Project Example

- Create VHDL file
  - Create a VHDL file for your schematic
  - Select File → Create/Update → Create HDL Design File from Current File

```
-- Copyright (C) 2017 Intel Corporation. All rights reserved.
-- Your use of Intel Corporation's design tools, logic functions
-- and other software and tools, and its AMPP partner logic
-- functions, and any output files from any of the foregoing
-- (including device programming or simulation files), and any
-- associated documentation or information are expressly subject
-- to the terms and conditions of the Intel Program License
-- Subscription Agreement, the Intel Quartus Prime License Agreement,
-- the Intel FPGA IP License Agreement, or other applicable license
-- agreement, including, without limitation, that your use is for
-- the sole purpose of programming logic devices manufactured by
-- Intel and sold by Intel or its authorized distributors. Please
-- refer to the applicable agreement for further details.
```

```
-- PROGRAM      "Quartus Prime"
-- VERSION      "Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition"
-- CREATED      "Fri Feb 23 15:52:47 2018"
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
```

```
LIBRARY work;
```

```
ENTITY MyFirstLogic IS
  PORT
  (
    in_A : IN STD_LOGIC;
    in_B : IN STD_LOGIC;
    out_1 : OUT STD_LOGIC;
    out_2 : OUT STD_LOGIC
  );
END MyFirstLogic;
```

```
ARCHITECTURE bdf_type OF MyFirstLogic IS
```

```
SIGNAL SYNTHESIZED_WIRE_12 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_13 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_14 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_4 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_8 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_9 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_10 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_11 : STD_LOGIC;
```

```
BEGIN
```

```
SYNTHESIZED_WIRE_11 <= SYNTHESIZED_WIRE_12 AND SYNTHESIZED_WIRE_13;
```

```
SYNTHESIZED_WIRE_13 <= NOT(in_A AND in_B);
```

```
SYNTHESIZED_WIRE_4 <= NOT(in_A OR in_B);
```

```
SYNTHESIZED_WIRE_12 <= in_B AND in_A;
```

```
SYNTHESIZED_WIRE_14 <= in_A OR in_B;
```

```
SYNTHESIZED_WIRE_9 <= SYNTHESIZED_WIRE_14 OR SYNTHESIZED_WIRE_12;
```

```
SYNTHESIZED_WIRE_10 <= SYNTHESIZED_WIRE_4 AND SYNTHESIZED_WIRE_14;
```

```
SYNTHESIZED_WIRE_8 <= SYNTHESIZED_WIRE_14 AND SYNTHESIZED_WIRE_13;
```

```
out_2 <= SYNTHESIZED_WIRE_8 OR SYNTHESIZED_WIRE_9;
```

```
out_1 <= SYNTHESIZED_WIRE_10 AND SYNTHESIZED_WIRE_11;
```

```
END bdf_type;
```



# Schematic Project Example

- Create VHDL file
  - Create a component template for your design (DUT)
    - Select **File** → **Create/Update** → **Create VHDL Component Declaration Files from Current File**

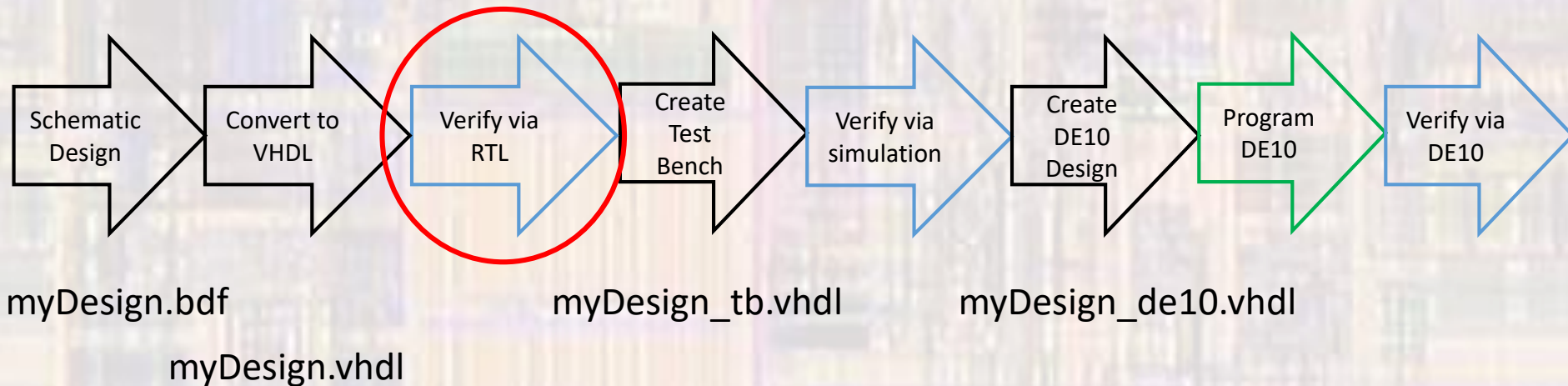
```
-- Copyright (C) 2017 Intel Corporation. All rights reserved.  
-- Your use of Intel Corporation's design tools, logic functions  
-- and other software and tools, and its AMPP partner logic  
-- functions, and any output files from any of the foregoing  
-- (including device programming or simulation files), and any  
-- associated documentation or information are expressly subject  
-- to the terms and conditions of the Intel Program License  
-- Subscription Agreement, the Intel Quartus Prime License Agreement,  
-- the Intel FPGA IP License Agreement, or other applicable license  
-- agreement, including, without limitation, that your use is for  
-- the sole purpose of programming logic devices manufactured by  
-- Intel and sold by Intel or its authorized distributors. Please  
-- refer to the applicable agreement for further details.
```

```
-- Generated by Quartus Prime Version 17.1 (Build Build 590 10/25/2017)  
-- Created on Fri Feb 23 15:57:28 2018
```

```
COMPONENT MyFirstLogic  
  PORT  
  (  
    in_A      : IN STD_LOGIC;  
    in_B      : IN STD_LOGIC;  
    out_1     : OUT STD_LOGIC;  
    out_2     : OUT STD_LOGIC  
  );  
END COMPONENT;
```

# Schematic Project Example

- Project Flow





# Schematic Project Example

- Create VHDL file
  - Prepare to use the VHDL file
    - Remove the BDF file from the project
      - In project Navigator – Files, Right click the BDF file and select:  
[Remove file from project](#)
    - Add the created VHDL file to the project
      - Select [Project](#) → [Add/remove files in project](#) → [file name ...](#)
      - Select the file to add
    - Set the VHDL file as the Top-Level Entity
      - In project Navigator – Files, Right click the VHDL file and select:  
[Set as Top-Level Entity](#)

# Schematic Project Example

- Create VHDL file
  - Verify your code is synthesizable
  - Select **Processing** -> **Start** -> **Start Analysis & Elaboration**

The screenshot shows the Quartus Prime Lite Edition interface. The 'Processing' menu is open, and the 'Start' option is selected, which has opened a sub-menu. In this sub-menu, 'Start Analysis & Elaboration' is highlighted with a red circle. Other options in the sub-menu include 'Start Hierarchy Elaboration', 'Start Analysis & Synthesis', 'Start Partition Merge', 'Start Fitter', 'Start Assembler', 'Start TimeQuest Timing Analyzer', 'Start EDA Netlist Writer', 'Start Design Assistant', 'Start Power Analyzer', 'Start SSN Analyzer', 'Start Rapid Recompile', 'Start Signal Probe Compilation', 'Start I/O Assignment Analysis', 'Start Check & Save All Netlist Changes', 'Start Equation Writer (Post-synthesis)', 'Start Equation Writer (Post-fitting)', 'Start Test Bench Template Writer', and 'Start EDA Synthesis'. The main window shows a VHDL file named 'MyFirstLogic.vhd' open, with the following code visible:

```
16 -- PROGRAM "Quartus Prime  
17 -- VERSION "Version 17.1.0  
18 -- CREATED "Fri Feb 23 15:5  
19  
20 LIBRARY ieee;  
21 USE ieee.std_logic_1164.all;  
22  
23 LIBRARY work;  
24  
25 ENTITY MyFirstLogic IS  
26 PORT
```

The Messages window at the bottom shows a successful message: 'Quartus Prime Netlist Viewers Preprocess was successful. 0'. The status bar at the bottom indicates 'System (3) Processing (20)' and 'Analyzes and elaborates all files in the hierarchy of the current top-level entity'.

# Schematic Project Example

- Create VHDL file
  - Check all Warnings and Errors

The screenshot displays the Quartus Prime Lite Edition interface. The 'Flow Summary' window is open, showing a 'Successful' status for the compilation. The status bar at the bottom indicates 'Quartus Prime Analysis & Elaboration was successful. 0 errors, 187 warnings'. A red circle highlights the 'All' button in the message list, and another red circle highlights the 'Successful' status in the flow summary. A yellow callout box contains the text: 'you will get a large number of warnings if you read in the qsf file – 1 for every unused pin'. A blue callout box points to the 'Successful' status with the text 'Successful'. Another blue callout box at the bottom left points to the message list with the text 'Highlight errors and warning'.

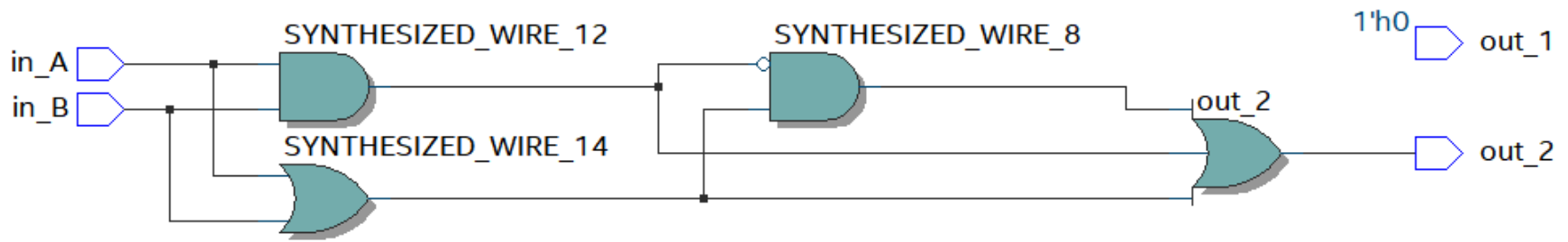
Successful

you will get a large number of warnings if you read in the qsf file – 1 for every unused pin

Highlight errors and warning

# Schematic Project Example

- Create VHDL file
  - **ALWAYS** check your RTL to make sure it makes sense
  - Select **Tools** → **Netlist Viewers** → **RTL Viewer**

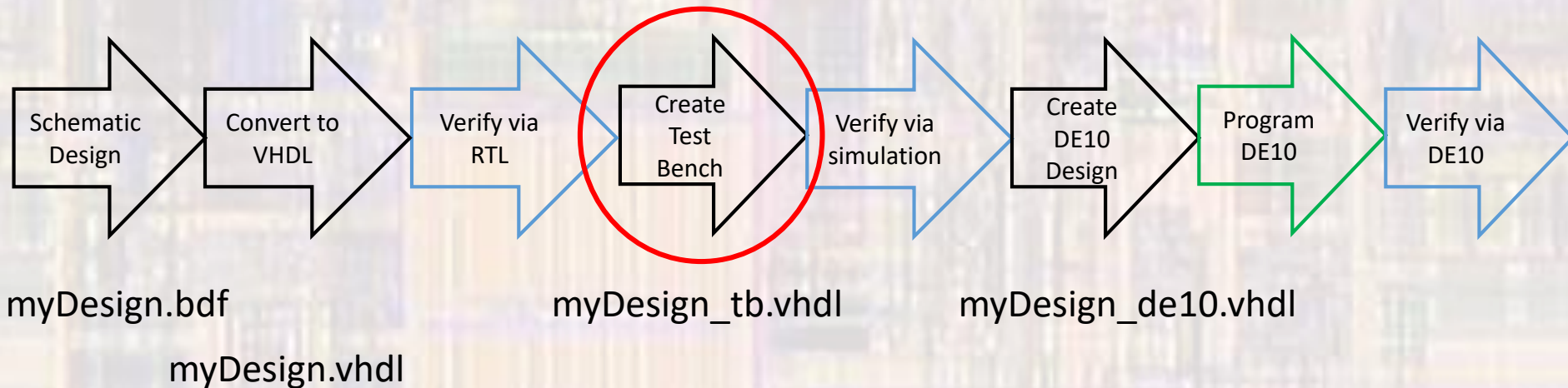


- Note – the new design will be optimized



# Schematic Project Example

- Project Flow





# Schematic Project Example

- Project Verification
  - Create a Test Bench
  - Open a new vhdl design file with the name MyFirstLogic\_tb
  - Create a test bench entity and instantiate your design at the device under test (DUT)
  - Create test inputs using the non-synthesizable `wait` instructions

# Schematic Project Example

- Project Verification
  - Create a Test Bench

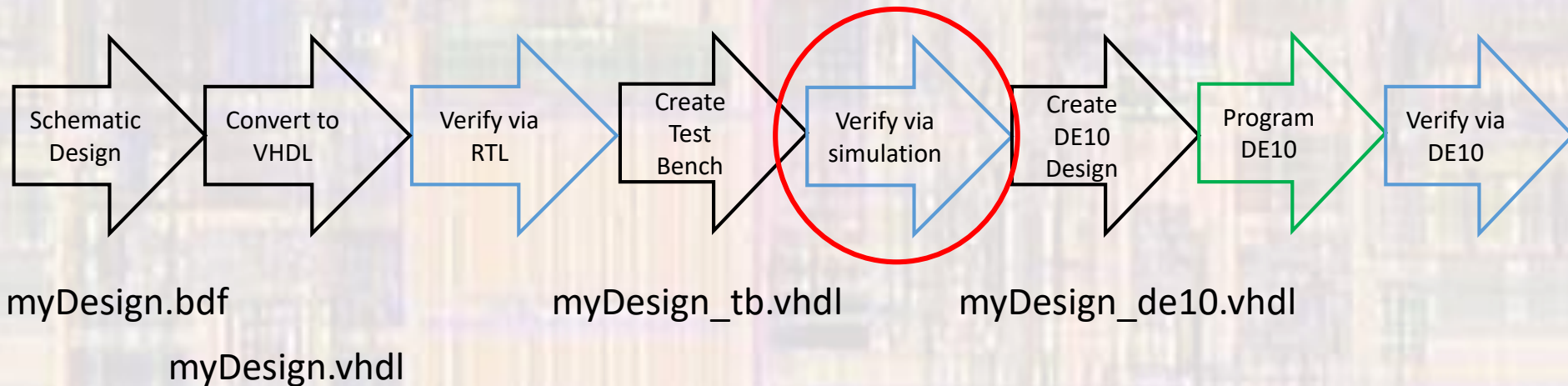
```
-----  
-- MyFirstLogic_tb.vhdl  
-- created: 1/26/18  
-- by: johnsontim  
-- rev: 0  
--  
-- testbench for logic example  
-- of MyFirstLogic.vhdl  
--  
-- brute force implementation  
-----  
library ieee;  
use ieee.std_logic_1164.all;  
entity MyFirstLogic_tb is  
  -- no entry - testbench  
end entity;
```

```
architecture testbench of MyFirstLogic_tb is  
  signal IN_A: std_logic;  
  signal IN_B: std_logic;  
  
  signal OUT_1: std_logic;  
  signal OUT_2: std_logic;  
  
  constant PER: time := 20 ns;  
  
  -----  
  -- Component prototype  
  -----  
  COMPONENT MyFirstLogic  
  PORT  
  (  
    in_A      : IN STD_LOGIC;  
    in_B      : IN STD_LOGIC;  
    out_1     : OUT STD_LOGIC;  
    out_2     : OUT STD_LOGIC  
  );  
  END COMPONENT;  
  
  -----
```

```
begin  
  
  -----  
  -- Device under test (DUT)  
  -----  
  DUT: MyFirstLogic  
  port map(  
    in_A => IN_A,  
    in_B => IN_B,  
    out_1 => OUT_1,  
    out_2 => OUT_2  
  );  
  
  -----  
  -- Brute force test process  
  -----  
  brute: process -- no sens|list allowed  
  begin  
    -----  
    -- Initialize all inputs  
    IN_A <= '0';  
    IN_B <= '0';  
    -----  
    -- run  
    wait for PER;  
    IN_A <= '1';  
    wait for PER;  
    IN_A <= '0';  
    wait for PER;  
    IN_B <= '1';  
    wait for PER;  
    IN_B <= '0';  
    wait for PER;  
    IN_A <= '1';  
    IN_B <= '1';  
    wait for PER;  
    IN_A <= '0';  
    IN_B <= '0';  
  end process brute;  
end architecture;
```

# Schematic Project Example

- Project Flow



# Schematic Project Example

- Project Verification
  - Elaborate the design
    - With the original vhdl design set as the top level entity (**not the xxxx\_tb.vhdl design**)
    - Select **Processing** → **Start** → **Start Analysis and Elaboration**
  - This causes Quartus to check the Test Bench code along with the original vhdl design

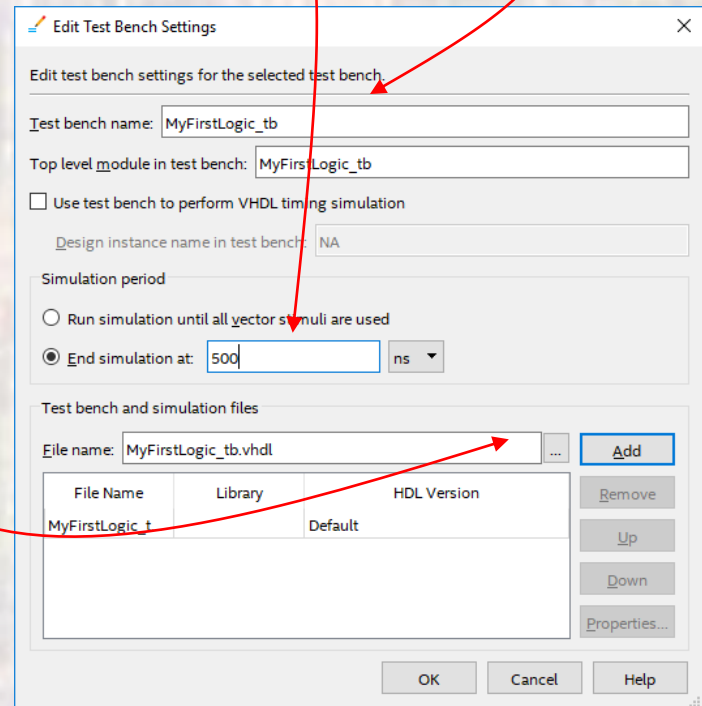
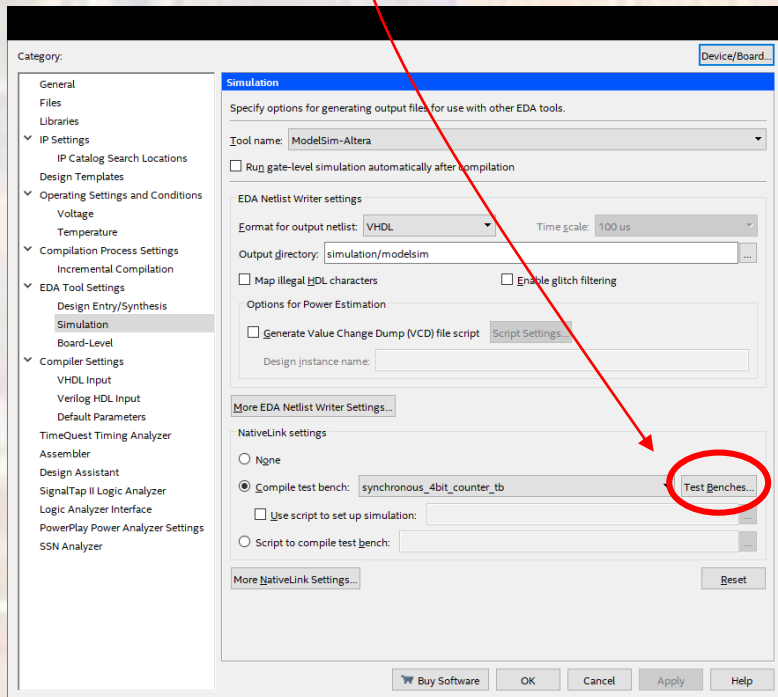


# Schematic Project Example

- Project Verification

- Setup the test bench

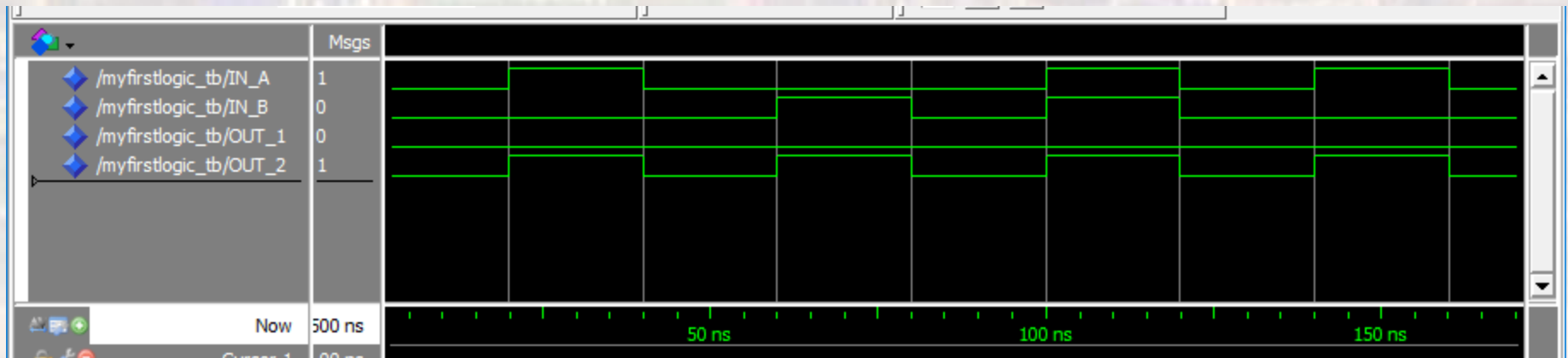
- Select **Assignments** → **Settings** → **EDA Tool Settings** → **Simulation** → **Test Benches** : enter the test bench file
- : select the end simulation time
- : select **File name ...** and select the test bench file





# Schematic Project Example

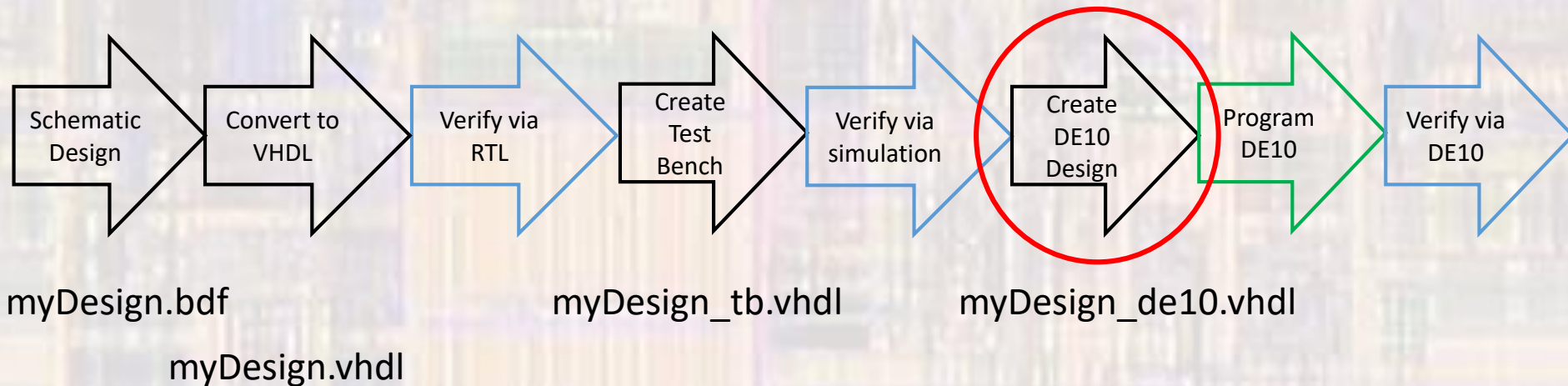
- Project Verification
  - Run the simulation
    - Select **Tools** → **Run Simulation Tool** → **RTL Simulation**



1 full cycle

# Schematic Project Example

- Project Flow



# Schematic Project Example

- Project Implementation
  - Prepare for DE10
  - Create a new VHDL File
    - MyFirstLogic\_de10.vhdl
  - Use the DE10 pin names from the qsf file
    - or you can use the pin planner
  - Instantiate your Design

# Schematic Project Example

- Project Implementation
  - Prepare for DE10

```
-----  
-- MyFirstLogic_de10.vhdl  
-- created: 2/23/18  
-- by: johnsontim  
-- rev: 0  
--  
-- DE10 file for random logic  
-- of MyFirstLogic.vhdl  
--  
-- using qsf pin names  
-- SW[0] --> in_A  
-- SW[1] --> in_B  
--  
-- LEDR --> Out_1 and out_2  
--  
-----  
library ieee;  
use ieee.std_logic_1164.all;  
  
entity MyFirstLogic_de10 is  
    PORT(  
        SW:          in std_logic_vector(1 downto 0);  
        LEDR:        out std_logic_vector(1 downto 0)  
    );  
end entity;
```

```
architecture testbench of MyFirstLogic_de10 is  
  
    -----  
    -- Component prototype  
    -----  
    COMPONENT MyFirstLogic  
    PORT  
    (  
        in_A      :    IN STD_LOGIC;  
        in_B      :    IN STD_LOGIC;  
        out_1     :    OUT STD_LOGIC;  
        out_2     :    OUT STD_LOGIC  
    );  
    END COMPONENT;  
  
    -----  
    begin  
  
    -----  
    -- Design placement  
    -----  
    DESIGN: MyFirstLogic  
    port map(  
        in_A => SW(0),  
        in_B => SW(1),  
        out_1 => LEDR(0),  
        out_2 => LEDR(1)  
    );  
  
end architecture;
```



# Schematic Project Example

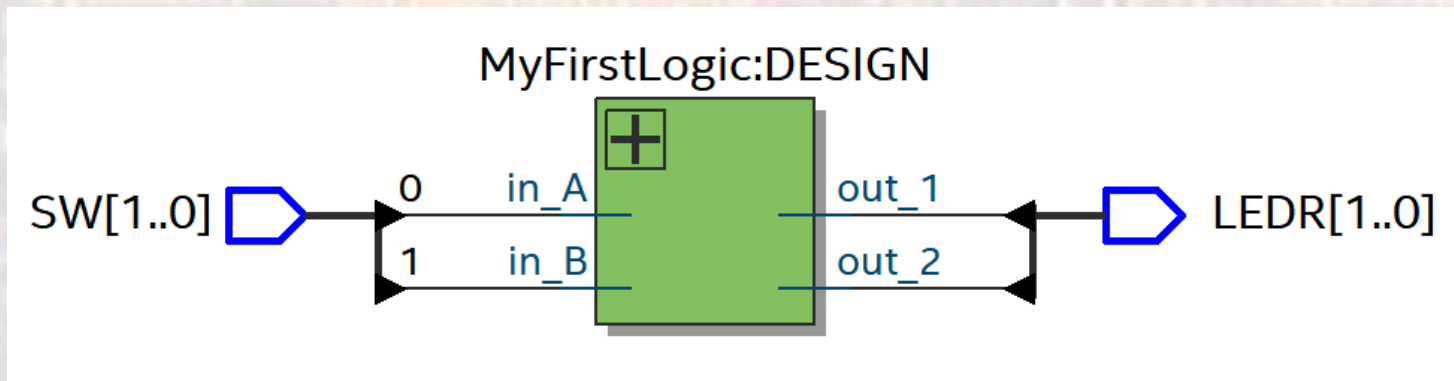
- Project Implementation
  - Prepare for DE10
  - Compile your design
  - Check the Compilation Summary

Flow Summary	
Flow Status	Successful - Fri Feb 23 17:01:47 2018
Quartus Prime Version	17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name	MyFirstDE10Project
Top-level Entity Name	MyFirstLogic_de10
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2 / 49,760 (< 1 %)
Total registers	0
Total pins	4 / 360 (1 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)



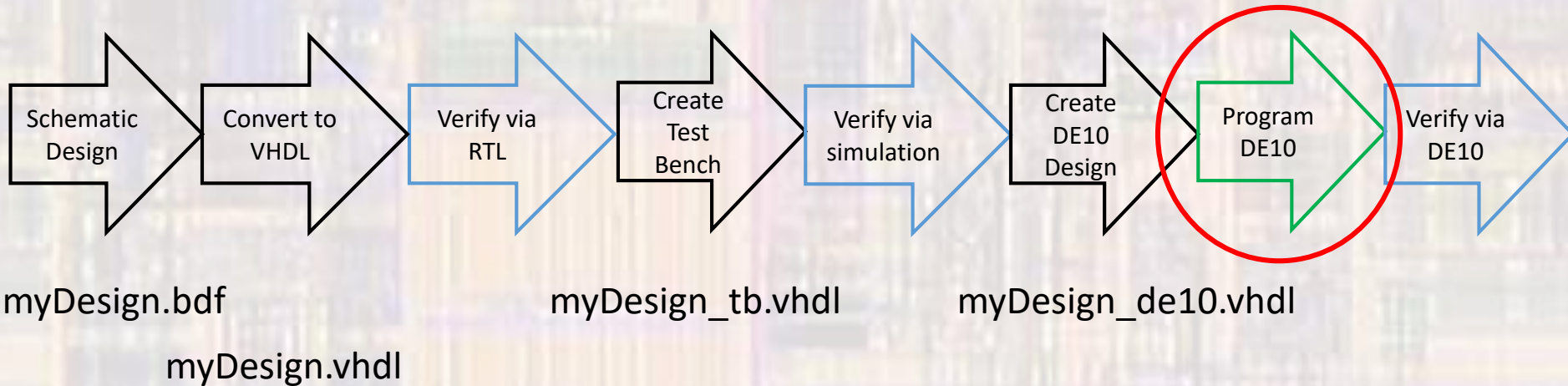
# Schematic Project Example

- Project Implementation
  - Prepare for DE10
  - Check the RTL



# Schematic Project Example

- Project Flow

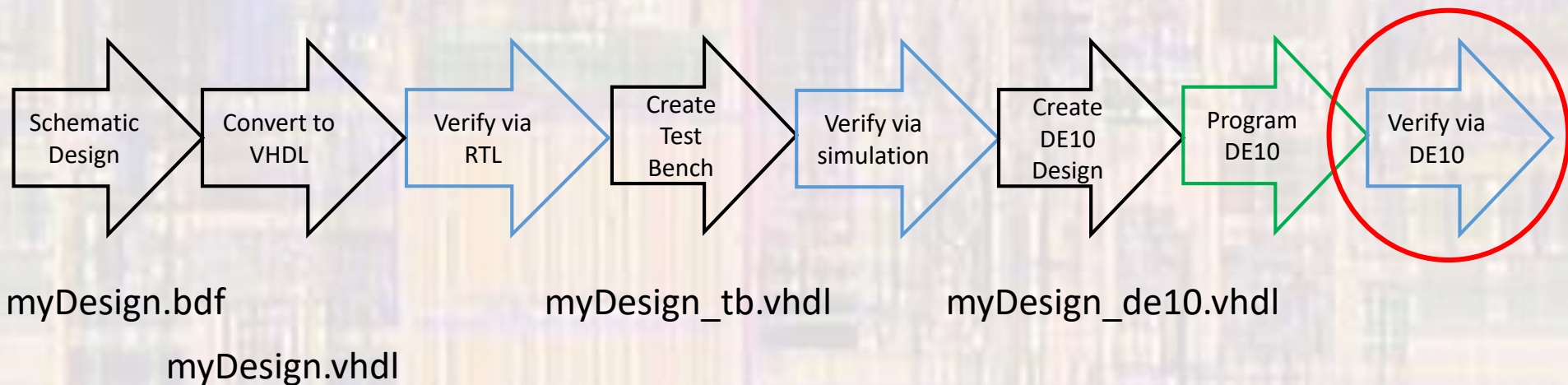


# Schematic Project Example

- Project Implementation
  - Configure the DE10
  - Select **Tools** -> **Programmer**
    - point to the compiled output file
    - start

# Schematic Project Example

- Project Flow





# Schematic Project Example

- Project Implementation
  - Configure the DE10
  - Validate the design on the DE10 board