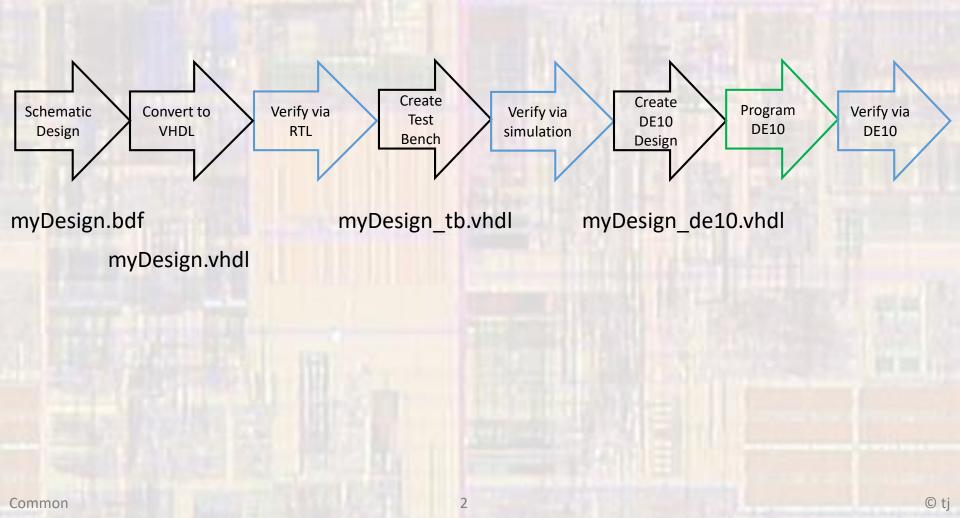
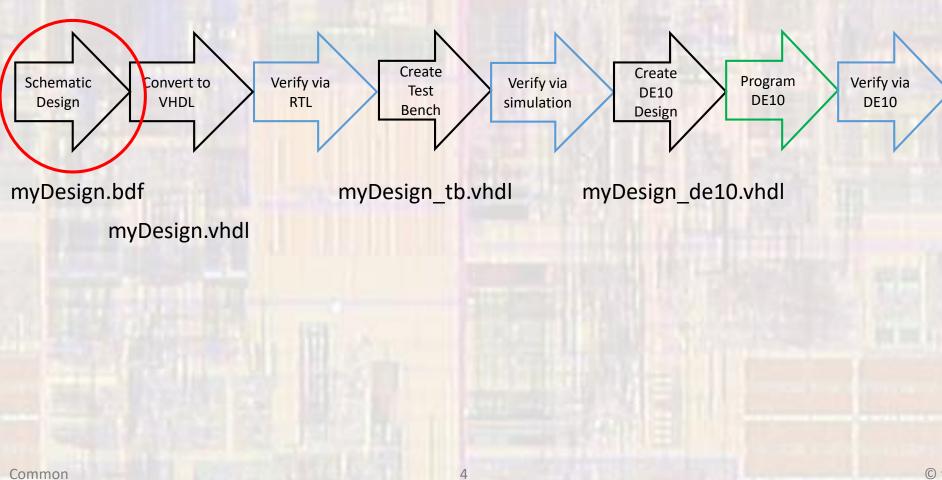
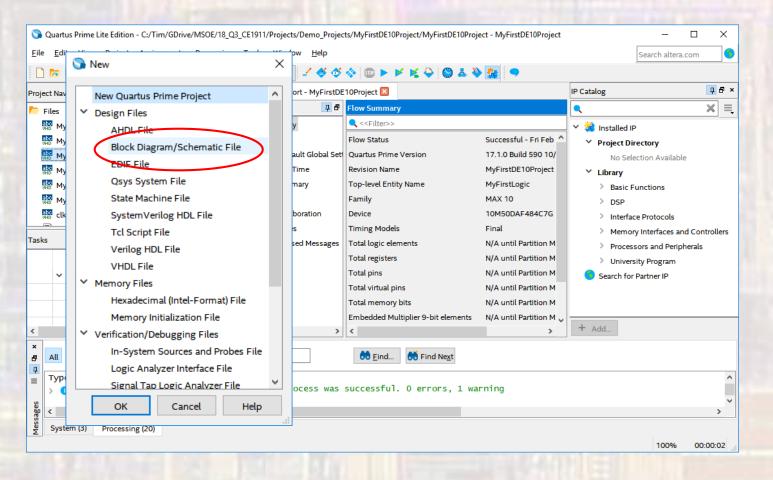
Common - last updated 2/11/19



- Create a new Project
  - Select File -> New Project Wizard
    - ...
    - See project setup slides if necessary



- Create a new BDF file
  - Select File -> New -> Block Diagram/Schematic File



- Create a new BDF file
  - Note the default file name
  - We want this to be our top level entity so we must change the name

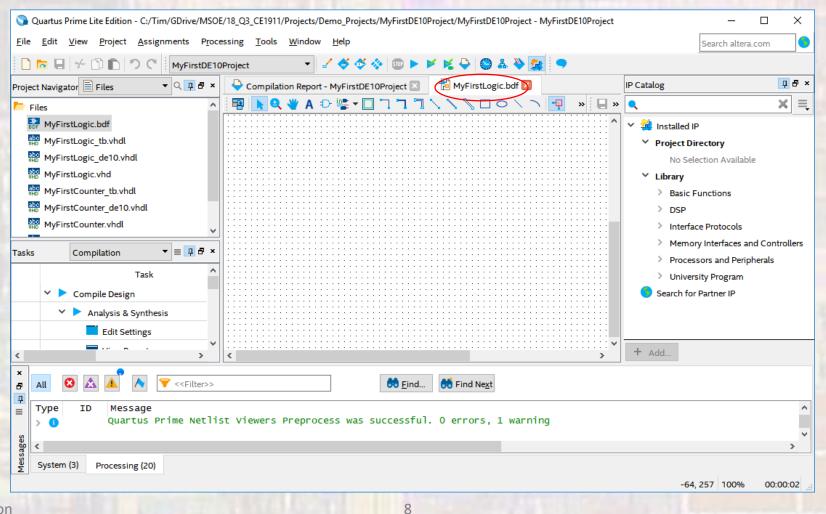
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- Create a new BDF file
  - Select File -> Save As
  - Set the file name to the our desired value
  - Make sure "Add file to current project" is checked

Save As					×
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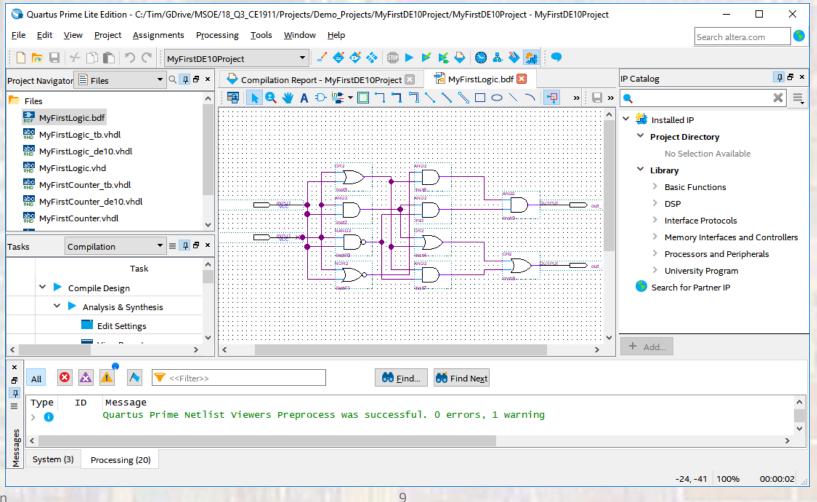
#### Create a new BDF file

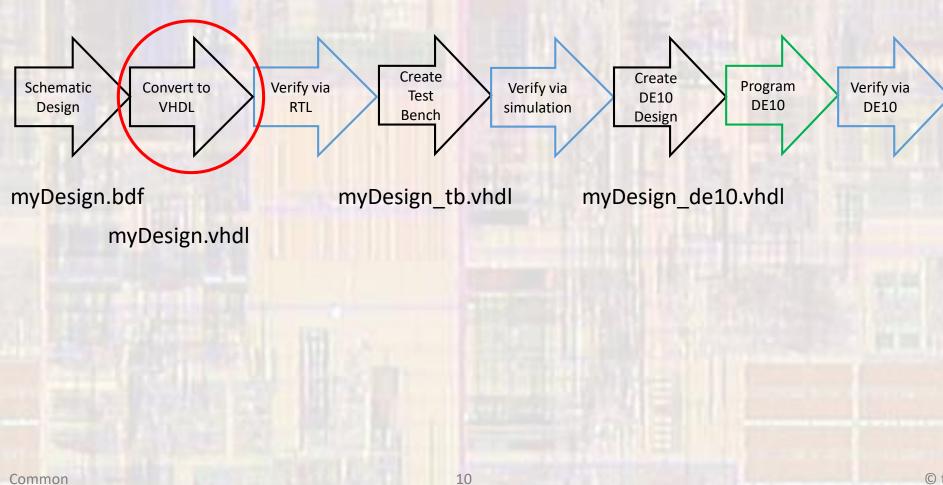
Note the name change



#### Create a new BDF file

Create your schematic





#### Create VHDL file

- Create a VHDL file for your schematic
- Select File → Create/Update → Create HDL Design File from Current File
   ARCHITECTURE bdf\_type OF MyFirstLogic IS

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-- PROGRAM "Quartus Prime"

-- VERSION "Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition" -- CREATED "Fri Feb 23 15:52:47 2018"

LIBRARY ieee; USE ieee.std\_logic\_1164.all;

#### LIBRARY work;

ENTITY MyFirstLogic IS PORT ( in\_A: IN STD\_LOGIC; in\_B: IN STD\_LOGIC; out\_1: OUT STD\_LOGIC; out\_2: OUT STD\_LOGIC ); END MyFirstLogic; SIGNAL SYNTHESIZED\_WIRE\_12: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_13: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_14: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_4: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_8: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_9: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_10: STD\_LOGIC; SIGNAL SYNTHESIZED\_WIRE\_11: STD\_LOGIC;

#### BEGIN

SYNTHESIZED\_WIRE\_11 <= SYNTHESIZED\_WIRE\_12 AND SYNTHESIZED\_WIRE\_13;

SYNTHESIZED\_WIRE\_13 <= NOT(in\_A AND in\_B);

SYNTHESIZED\_WIRE\_4 <= NOT(in\_A OR in\_B);</pre>

SYNTHESIZED\_WIRE\_12 <= in\_B AND in\_A;

SYNTHESIZED\_WIRE\_14 <= in\_A OR in\_B;

SYNTHESIZED\_WIRE\_9 <= SYNTHESIZED\_WIRE\_14 OR SYNTHESIZED\_WIRE\_12;

SYNTHESIZED\_WIRE\_10 <= SYNTHESIZED\_WIRE\_4 AND SYNTHESIZED\_WIRE\_14;

SYNTHESIZED\_WIRE\_8 <= SYNTHESIZED\_WIRE\_14 AND SYNTHESIZED\_WIRE\_13;

out\_2 <= SYNTHESIZED\_WIRE\_8 OR SYNTHESIZED\_WIRE\_9;</pre>

out\_1 <= SYNTHESIZED\_WIRE\_10 AND SYNTHESIZED\_WIRE\_11;</pre>

END bdf\_type;

#### Create VHDL file

- Create a component template for your design (DUT)
  - Select File → Create/Update → Create VHDL Component Declaration Files from Current File
- -- Copyright (C) 2017 Intel Corporation. All rights reserved.
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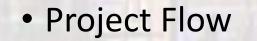
-- Generated by Quartus Prime Version 17.1 (Build Build 590 10/25/2017)

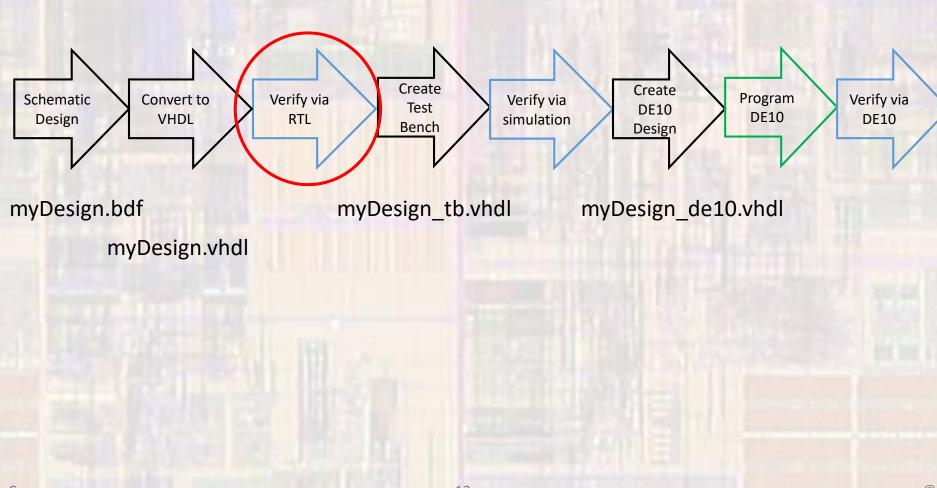
-- Created on Fri Feb 23 15:57:28 2018

#### COMPONENT MyFirstLogic PORT

EN

in_A	:	IN STD_LOGIC;
in_B	:	IN STD_LOGIC;
out_1	:	OUT STD_LOGIC;
out_2	:	OUT STD_LOGIC
);		
D COMPONE	NT;	





- Create VHDL file
  - Prepare to use the VHDL file
    - Remove the BDF file from the project
      - In project Navigator Files, Right click the BDF file and select: Remove file from project
    - Add the created VHDL file to the project
      - Select Project → Add/remove files in project → file name ...
      - Select the file to add
    - Set the VHDL file as the Top-Level Entity
      - In project Navigator Files, Right click the VHDL file and select: Set as Top-Level Entity

#### • Create VHDL file

- Verify your code is synthesizable
- Select Processing -> Start -> Start Analysis & Elaboration

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▶ Files	2	Analyze Current File	8	2	٩	× =
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MyFirstLogic_de10.vhdl	•	Update Memory Initialization File Compilation Report Ctrl+R	Ķ	Start Analysis & Elaboration	Ctrl+K	i <b>rectory</b> ection Available
MyFirstCounter_tb.vhdl	↓ <i>≠</i> ₩	Dynamic Synthesis Report Power Analyzer Tool SSN Analyzer Tool	74 111 111 111	Start Partition Merge Start Fitter Start Assembler		Functions
Tasks Compilation ▼ = ₽		Receive Compilation Status Notifications		Start TimeQuest Timing Analyzer Start EDA Netlist Writer Start Design Assistant	Ctrl+Shift+T	ce Protocols ry Interfaces and Controllers sors and Peripherals
Task Compile Design Analysis & Synthesis	_	18 L 19 LIBRARY ieee; 20 USE ieee.std_logic_1164.all; 21	<b>≯</b>	Start Power Analyzer Start SSN Analyzer	Ctrl+Shift+P	sity Program <sup>,</sup> Partner IP
Edit Settings	_	22     LIBRARY work;       23     □       24     □       25     □       25     □	2	Start Rapid Recompile		-
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Common

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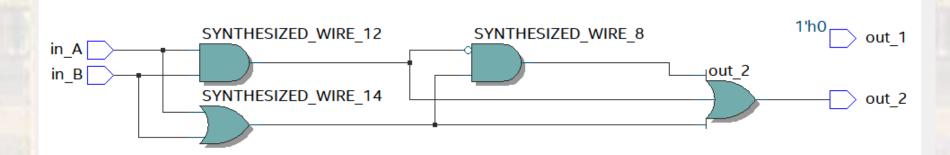
#### Create VHDL file

Check all Warnings and Errors

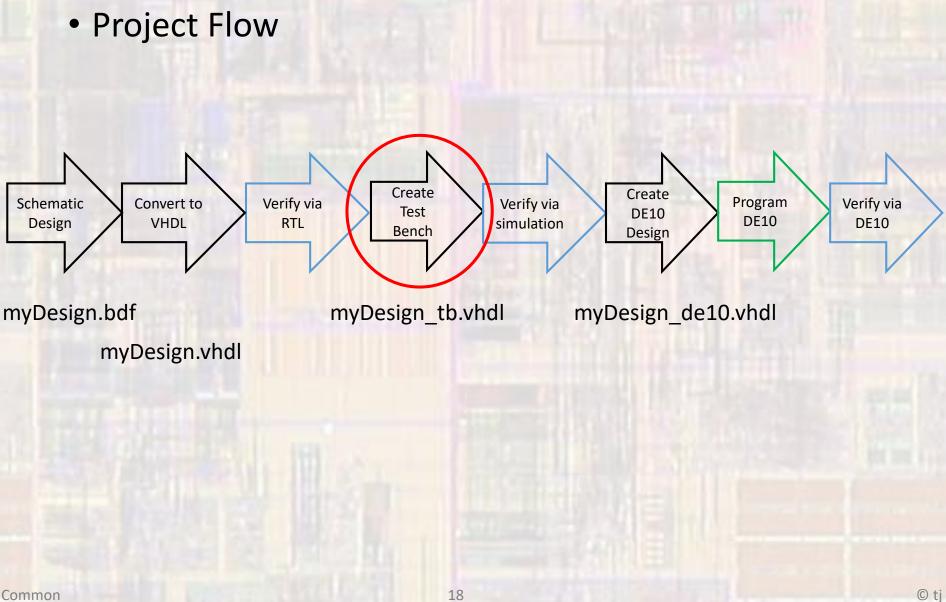
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MyFirstLogic_de10.vhdl	Flow Settings	Flow Status	Successful - Fri Feb ^	Y Project Directory	
MyFirstLogic.vhd	Flow Non-Default Global Set	Quartus Prime Version	17.1.0 Build 590 10/	No Selection Available	
abo MyFirstCounter_tb.vhdl	Flow Elapsed Time	Revision Name Flow S	Status irstDE10Project	✓ Library	
MyFirstCounter_de10.vhdl		Top-level Entity Name	MyFirstLogic	Basic Functions	
MyFirstCounter.vhdl	Flow Log	Family	MAX 10	> DSP	
elk10Hz.vhdl	> Analysis & Elaboration	Device	10M50DAF484C7G	> Interface Protocols	
		Timing Models	Final	Memory Interfaces and Controllers	
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V > Compile Design	-	Total pins	N/A until Partition M	Search for Partner IP	
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Successful

- Create VHDL file
  - ALWAYS check your RTL to make sure it makes sense
  - Select Tools → Netlist Viewers → RTL Viewer



Note – the new design will be optimized



- Project Verification
  - Create a Test Bench
  - Open a new vhdl design file with the name MyFirstLogic\_tb
  - Create a test bench entity and instantiate your design at the device under test (DUT)
  - Create test inputs using the non-synthesizable wait instructions

- Project Verification
  - Create a Test Bench

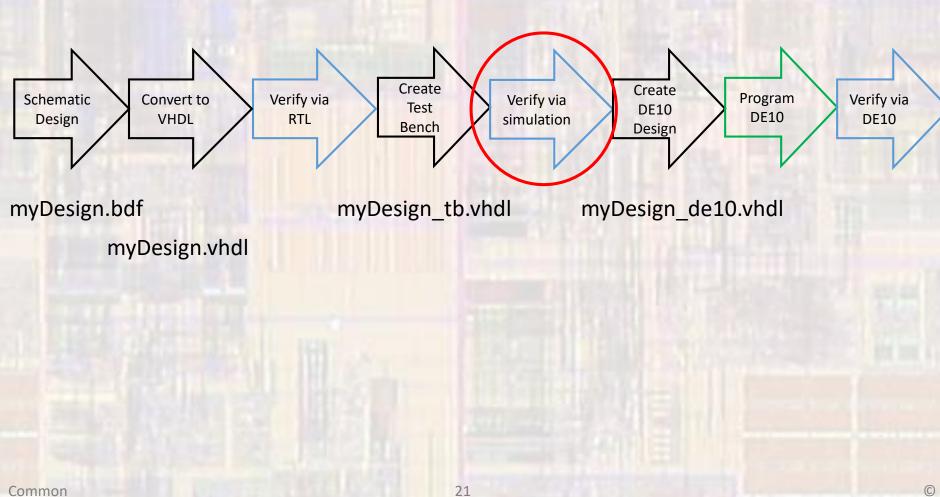
MyFirstLogic_tb.vhdl
created: 1/26/18 by: johnsontimoj rev: 0
testbench forlogic example of MyFirstLogic.vhdl
brute force implementation 
library ieee; use ieee.std_logic_1164.all;
<pre>entity MyFirstLogic_tb is     no entry - testbench end entity;</pre>

architecture testbench of MyFirstLogic_tb is signal IN_A: std_logic; signal IN_B: std_logic;
<pre>signal OUT_1: std_logic; signal OUT_2: std_logic;</pre>
<pre>constant PER: time := 20 ns;</pre>
Component prototype
COMPONENT MyFirstLogic
( in_A : IN STD_LOGIC; in_B : IN STD_LOGIC; out_1 : OUT STD_LOGIC; out_2 : OUT STD_LOGIC
); END COMPONENT;

<pre> Device under test (DUT) DUT: MyFirstLogic port map(</pre>	segn
<pre>port map(</pre>	Device under test (DUT)
<pre>in_A =&gt; IN_A, in_B =&gt; IN_B, out_1 =&gt; OUT_1, out_2 =&gt; OUT_2 );  Brute force test process brute: process no sens  list allowed begin  Initialize all inputs IN_A &lt;= '0'; IN_B &lt;= '0'; IN_B &lt;= '0'; IN_A &lt;= '0'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_A &lt;= '0'; mait for PER; IN_B &lt;= '0'; wait for PER; N_B &lt;= '0'; N_B &lt;=</pre>	
<pre>out_1 =&gt; OUT_1, out_2 =&gt; OUT_2 );  Brute force test process brute: process no sens  list allowed begin  Initialize all inputs IN_A &lt;= '0'; IN_B &lt;= '0'; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; and for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; and for PER; and for PER;</pre>	
<pre>out_2 =&gt; OUT_2 );  Brute force test process brute: process no sens  list allowed begin  Initialize all inputs IN_A &lt;= '0'; IN_B &lt;= '0';  run wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; end process brute;</pre>	$1n_B => IN_B,$ out_1 => OUT_1,
<pre> Brute force test process brute: process no sens  list allowed begin  Initialize all inputs IN_A &lt;= '0'; IN_B &lt;= '0';  run wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; at for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0';</pre>	$out_2 \implies OUT_2$
<pre>brute: process no sens  list allowed begin  Initialize all inputs IN_A &lt;= '0'; IN_B &lt;= '0';  run wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '1'; Wait for PER; IN_B &lt;= '1'; Wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0';</pre>	),
<pre>brute: process no sens  list allowed begin  Initialize all inputs IN_A &lt;= '0'; IN_B &lt;= '0';  run wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '1'; Wait for PER; IN_B &lt;= '1'; Wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0';</pre>	
<pre>begin     Initialize all inputs     IN_A &lt;= '0';     IN_B &lt;= '0';     IN_B &lt;= '0';     run     wait for PER;     IN_A &lt;= '1';     wait for PER;     IN_A &lt;= '0';     wait for PER;     IN_B &lt;= '1';     wait for PER;     IN_B &lt;= '0';     wait for PER;     IN_B &lt;= '1';     wait for PER;     IN_B &lt;= '0';     IN_B &lt;= '0';</pre>	Brute force test process
<pre>IN_A &lt;= '0'; IN_B &lt;= '0';  run wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_B &lt;= '0'; end process brute;</pre>	
<pre>IN_B &lt;= '0';  run wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	Initialize all inputs
run wait for PER; IN_A <= '1'; wait for PER; IN_B <= '0'; wait for PER; IN_B <= '0'; wait for PER; IN_B <= '0'; wait for PER; IN_A <= '1'; IN_B <= '1'; wait for PER; IN_A <= '0'; IN_B <= '0'; end process brute;	IN_A <= '0'; IN_B <= '0'
<pre>wait for PER; IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; iN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	
<pre>IN_A &lt;= '1'; wait for PER; IN_A &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; IN_B &lt;= '0';</pre>	wait for PER:
<pre>IN_A &lt;= '0'; wait for PER; IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; Wait for PER; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0';</pre>	IN_A <= '1';
<pre>IN_B &lt;= '1'; wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	IN_A <= '0':
<pre>wait for PER; IN_B &lt;= '0'; wait for PER; IN_A &lt;= '1'; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	wait for PER; TN B <= '1':
<pre>wait for PER; IN_A &lt;= '1'; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	wait for PER;
<pre>IN_A &lt;= '1'; IN_B &lt;= '1'; wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	IN_B <= '0'; wait for PER:
<pre>wait for PER; IN_A &lt;= '0'; IN_B &lt;= '0'; end process brute;</pre>	$TN \Delta \leq 1'$
<pre>IN_B &lt;= '0'; end process brute;</pre>	wait for PER;
end process brute;	
a architecture,	end process brute; d architecture;

begin

er



- Project Verification
  - Elaborate the design
    - With the original vhdl design set as the top level entity (not the xxxx\_tb.vhdl design)
    - Select Processing → Start → Start Analysis and Elaboration
  - This causes Quartus to check the Test Bench code along with the original vhdl design

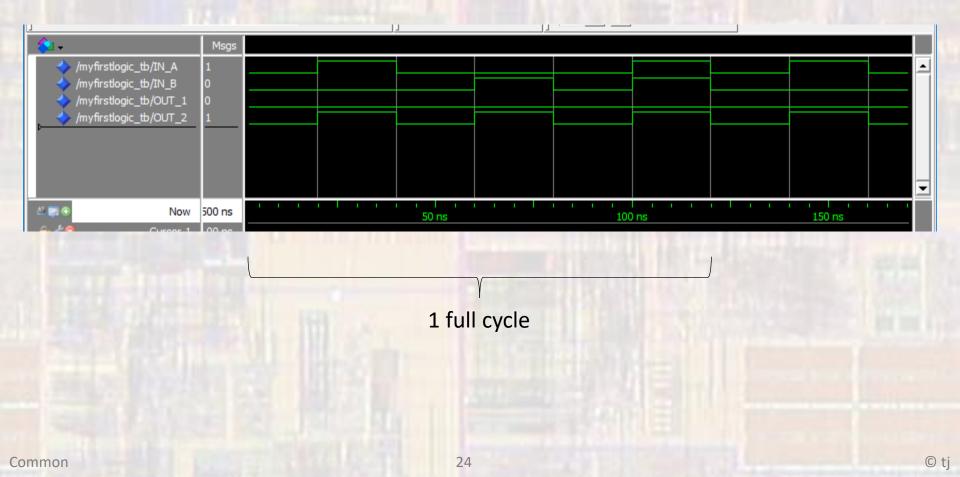
- Project Verification
  - Setup the test bench
    - Select Assignments → Settings → EDA Tool Settings →
       Simulation → Test Benches : enter the test bench file
      - : select the end simulation time
      - : select File name ... and select the test bench file

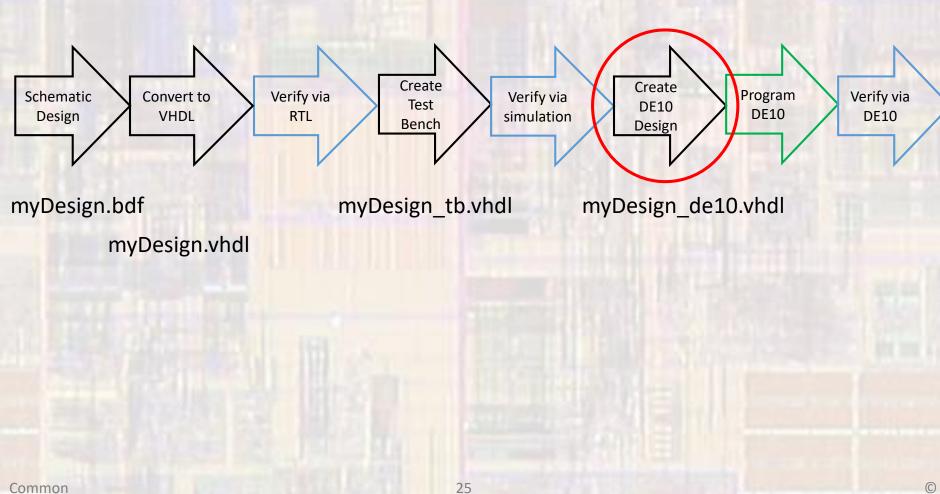
Category:	Device/Board
General	Simulation
Files	Specify options for generating output file, for use with other EDA tools.
Libraries	
✓ IP Settings	Tool name: ModelSim-Altera
IP Catalog Search Locations Design Templates	Run gate-level simulation automatically after compilation
✓ Operating Settings and Conditions	EDA Netlist Writer settings
Voltage Temperature	Eormat for output netlist: VHDL Time scale: 100 us
<ul> <li>Compilation Process Settings</li> </ul>	Output girectory: simulation/modelsim
Incremental Compilation	
✓ EDA Tool Settings	Map illegal HDL characters     Enable glitch filtering
Design Entry/Synthesis	Options for Power Estimation
Simulation	Generate Value Change Dump (VCD) file script Script Settings.
Board-Level	Generate value change bump (vcb) ne script - Script Settings
✓ Compiler Settings	Design instance name:
VHDL Input	
Verilog HDL Input	More EDA Netlist Writer Settings
Default Parameters	NativeLink settings
TimeQuest Timing Analyzer Assembler	wadveLink setungs
Design Assistant	O None
SignalTap II Logic Analyzer	Compile test bench: synchronous 4bit counter tb     Test Benches
Logic Analyzer Interface	Use script to set up simulation:
PowerPlay Power Analyzer Settings	
SSN Analyzer	O Script to compile test bench:
	More NativeLink Settings
	W Buy Software OK Cancel Apply Help

Edit Test Bench Settings	×	
Edit test bench settings for the selected test bench.		
Test bench name: MyFirstLogic_tb		
Top level <u>m</u> odule in test bench: MyFirs Logic_tb		
Use test bench to perform VHDL timing simulation		
Design instance name in test bench		
Simulation period		
O Run simulation until all vector stanuli are used		
● <u>E</u> nd simulation at: 500 ns ▼		
Test bench and simulation files		
Eile name: MyFirstLogic_tb.vhdl	<u>A</u> dd	
File Name Library HDL Version	<u>R</u> emove	
MyFirstLogic_t Default	Up	
	Down	
	Properties	
	Troperator	
OK Cancel	Help	

© ti

- Project Verification
  - Run the simulation
    - Select Tools → Run Simulation Tool → RTL Simulation

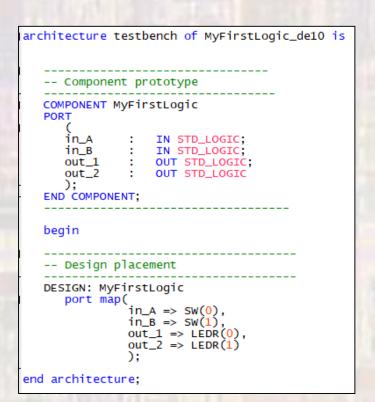




- Project Implementation
  - Prepare for DE10
  - Create a new VHDL File
    - MyFirstLogic\_de10.vhdl
  - Use the DE10 pin names from the qsf file
    - or you can use the pin planner
  - Instantiate your Design

- Project Implementation
  - Prepare for DE10

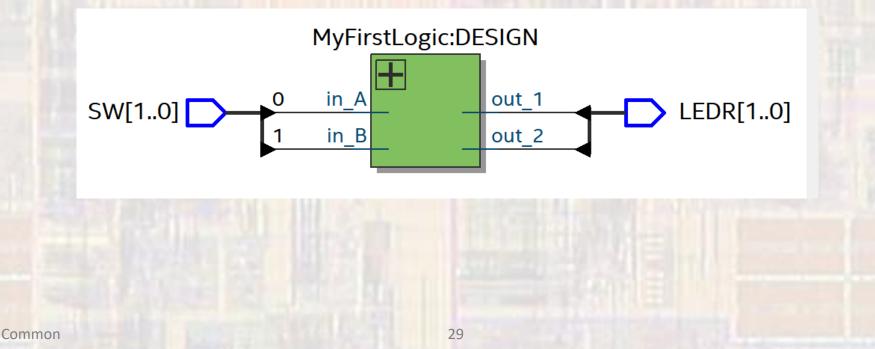
MyFirstLogic_d	e10.vhdl
	10
created: 2/23/3 by: johnsontim	
rev: 0	5)
DE10 file for I of MyFirstLogi	
OF MYFITSELOGIN	c. viui
using qsf pin i	names
SW[0]> in_A	
SW[1]> in_B 	
LEDR> Out_1	and out_2
library ieee;	
use ieee.std_logi	c_1164.all;
entity MyFirstLog PORT(	1C_del0 1S
SW:	<pre>in std_logic_vector(1 downto 0)</pre>
LEDR:	out std_logic_vector(1 downto 0)
);	
end entity;	

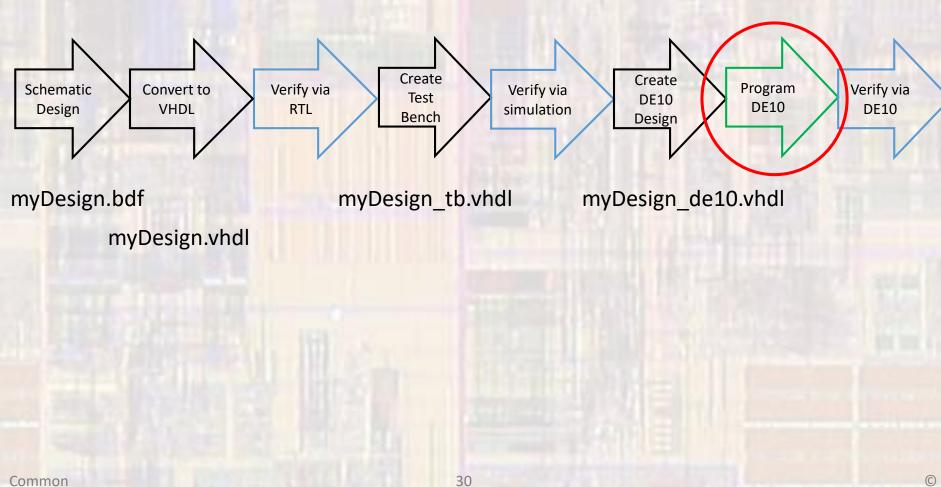


- Project Implementation
  - Prepare for DE10
  - Compile your design
  - Check the Compilation Summary

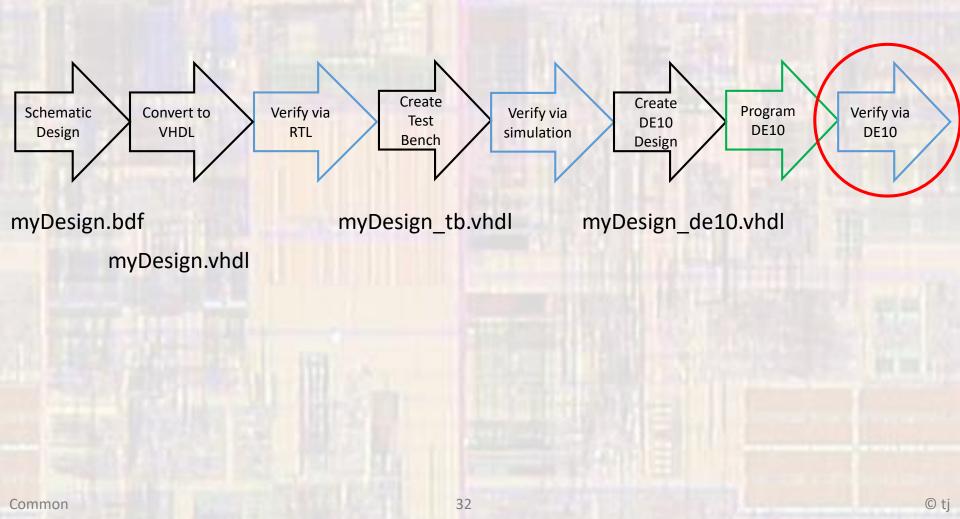
Flow Summary	
	$\sim$
Flow Status	Successful - ri Feb 23 17:01:47 2018
Quartus Prime Version	17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name	MyFirstDE10Project
Top-level Entity Name	MyFirstLogic_de10
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2 (49,760 ( < 1 % )
Total registers	0
Total pins	4 / 360 (1 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0%)
Embedded Multiplier 9-bit elements	0 / 288 ( 0 % )
Total PLLs	0/4(0%)
UFM blocks	0/1(0%)
ADC blocks	0/2(0%)

- Project Implementation
  - Prepare for DE10
  - Check the RTL





- Project Implementation
  - Configure the DE10
  - Select Tools -> Programmer
    - point to the compiled output file
    - start



- Project Implementation
  - Configure the DE10
  - Validate the design on the DE10 board