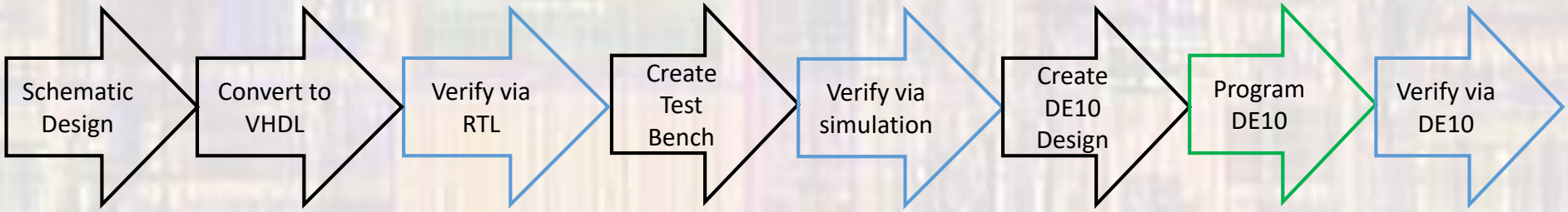
Schematic Project Example

Common - last updated 2/11/19

Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

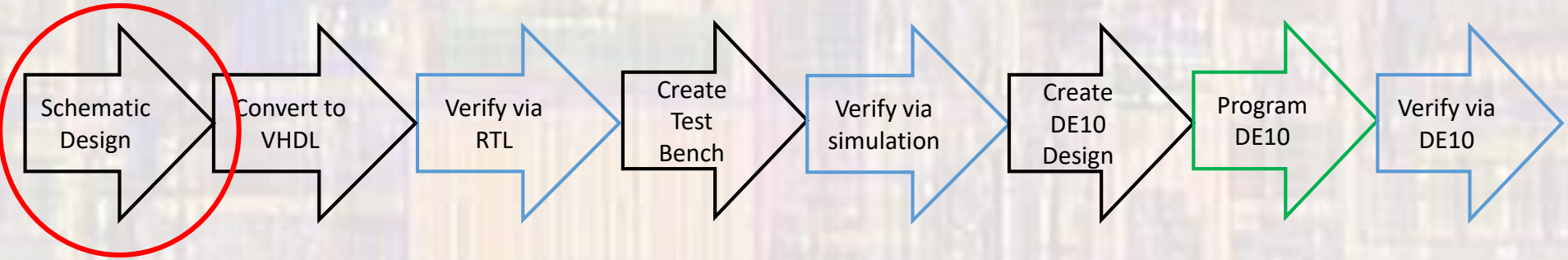
myDesign_de10.vhdl

Schematic Project Example

- Create a new Project
  - Select File -> New Project Wizard
    - …
    - See project setup slides if necessary

Schematic Project Example

- Project Flow



myDesign.bdf

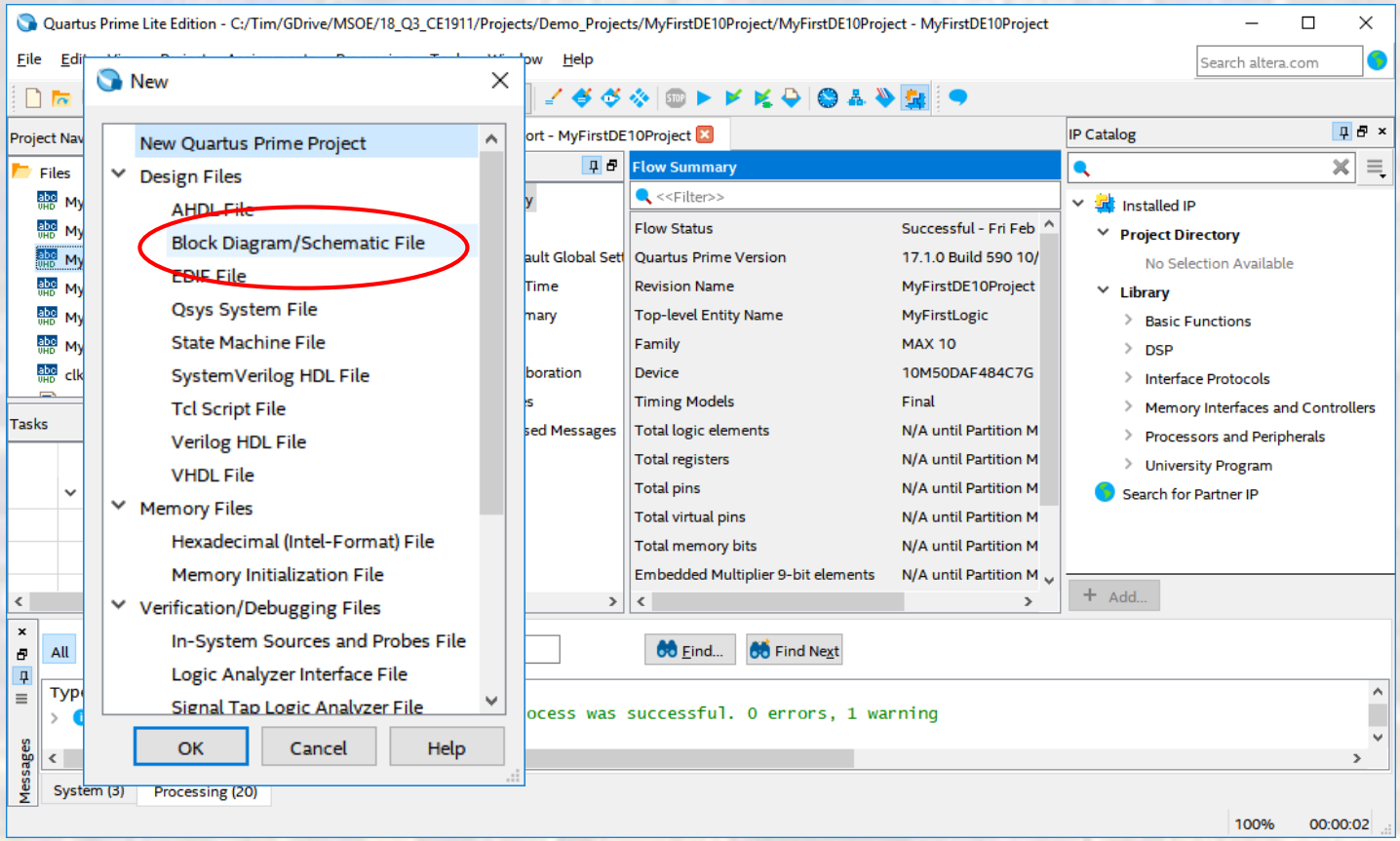
myDesign.vhdl

myDesign_tb.vhdl

myDesign_de10.vhdl

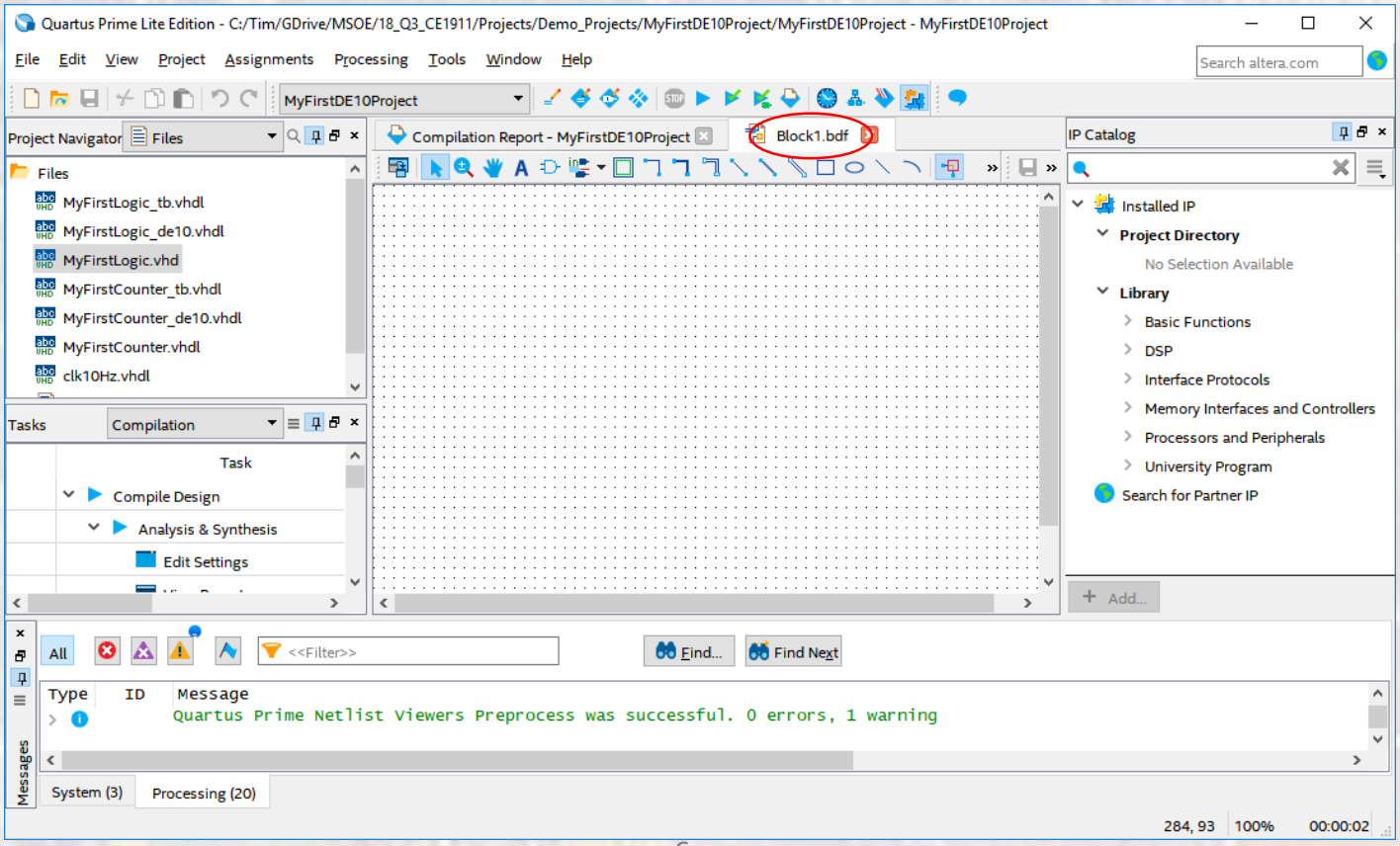
Schematic Project Example

- Create a new BDF file
  - Select File -> New -> Block Diagram/Schematic File



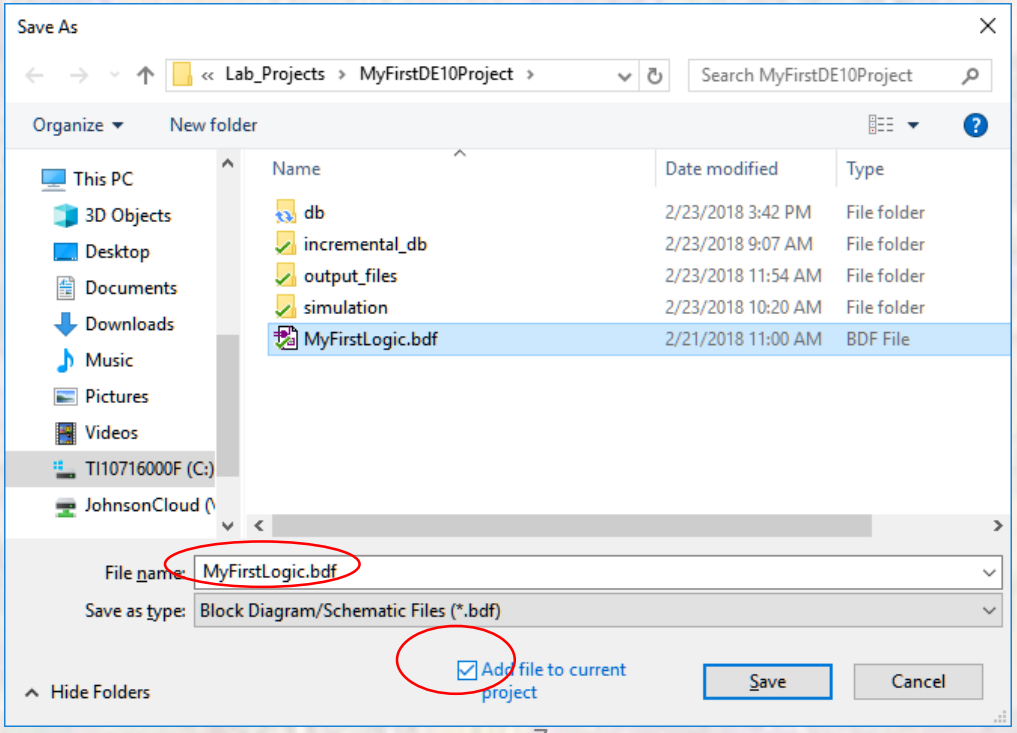
Schematic Project Example

- Create a new BDF file
  - Note the default file name
  - We want this to be our top level entity so we must change the name



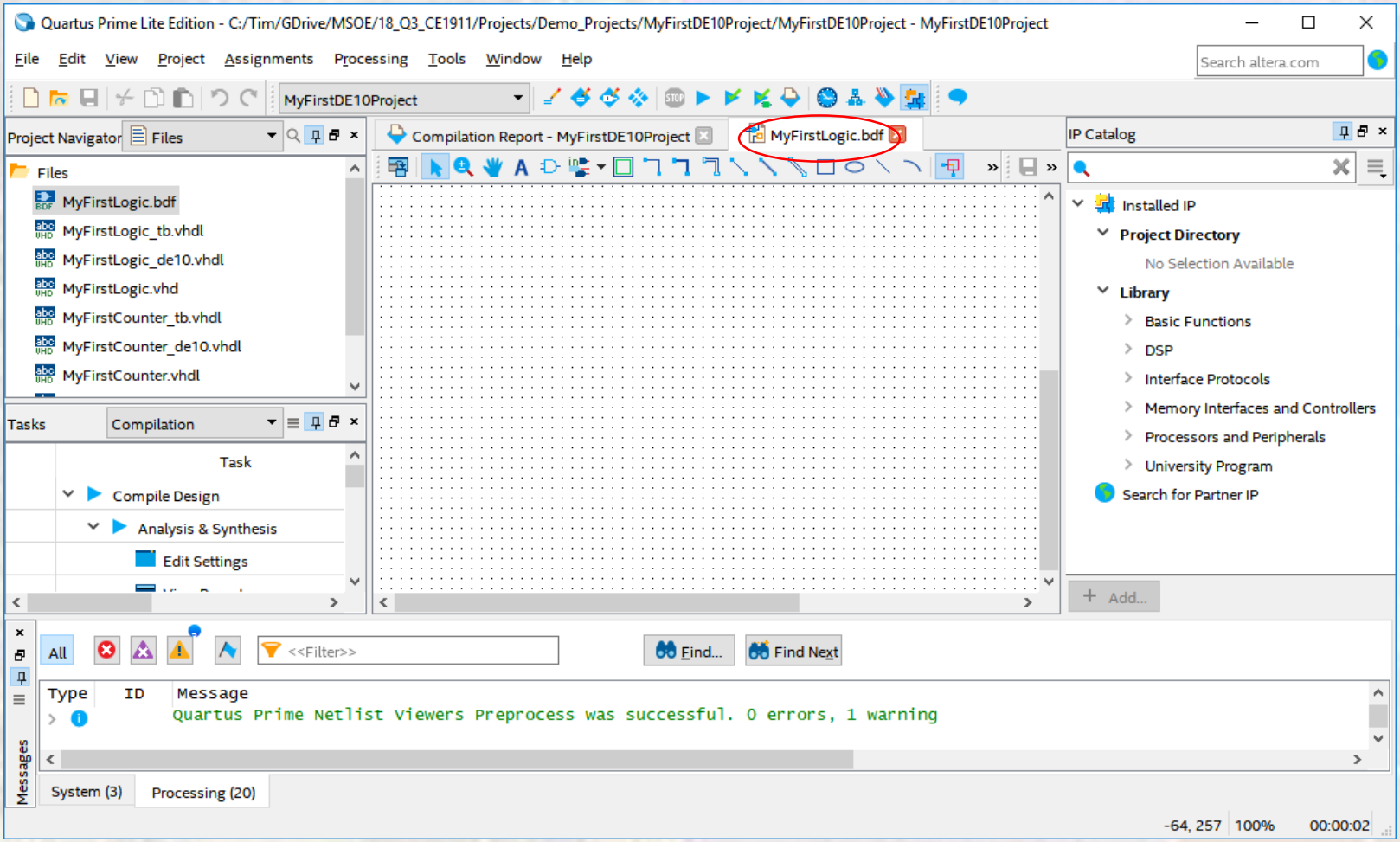
Schematic Project Example

- Create a new BDF file
  - Select File -> Save As
  - Set the file name to the our desired value
  - Make sure "Add file to current project" is checked



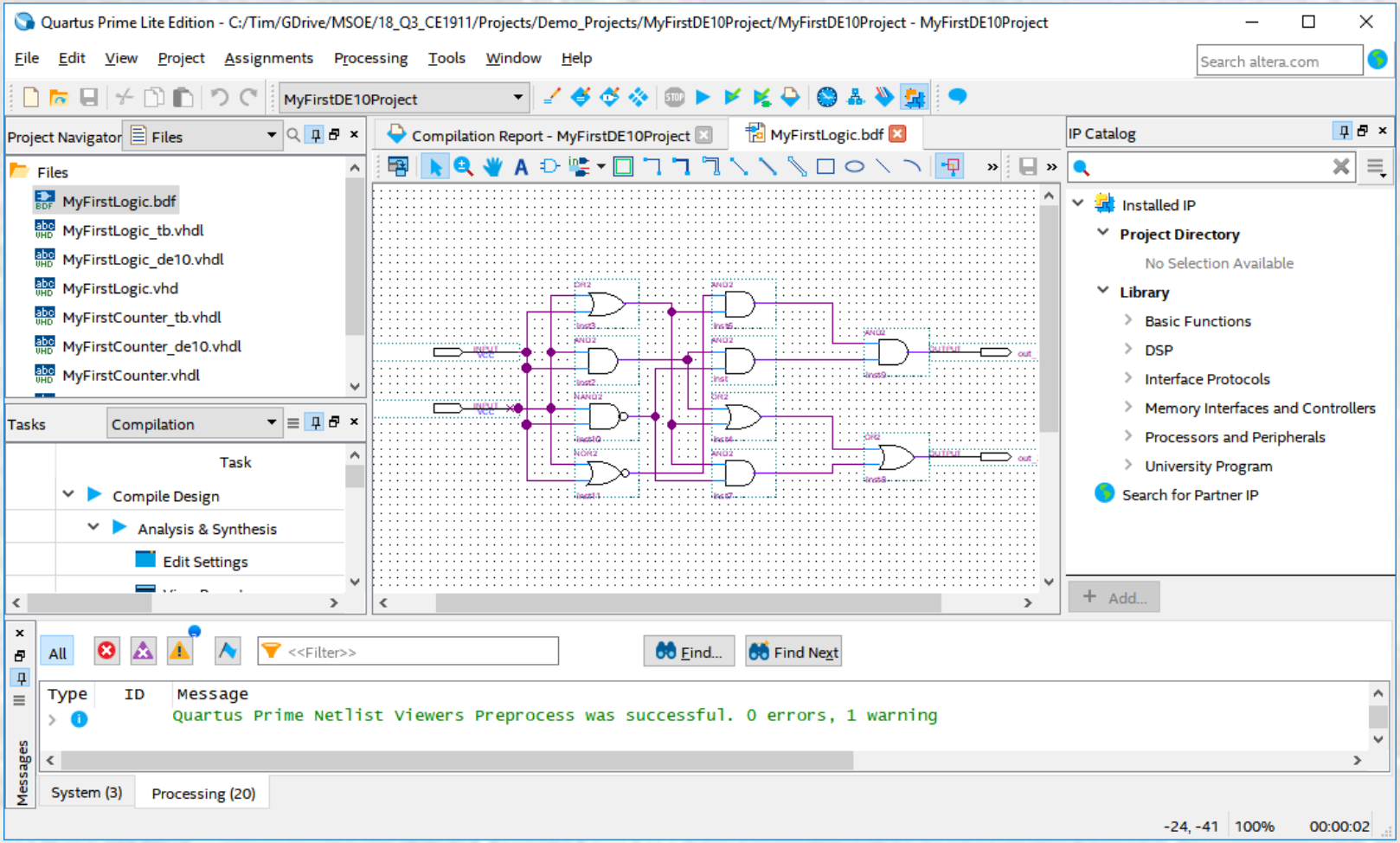
Schematic Project Example

- Create a new BDF file
  - Note the name change



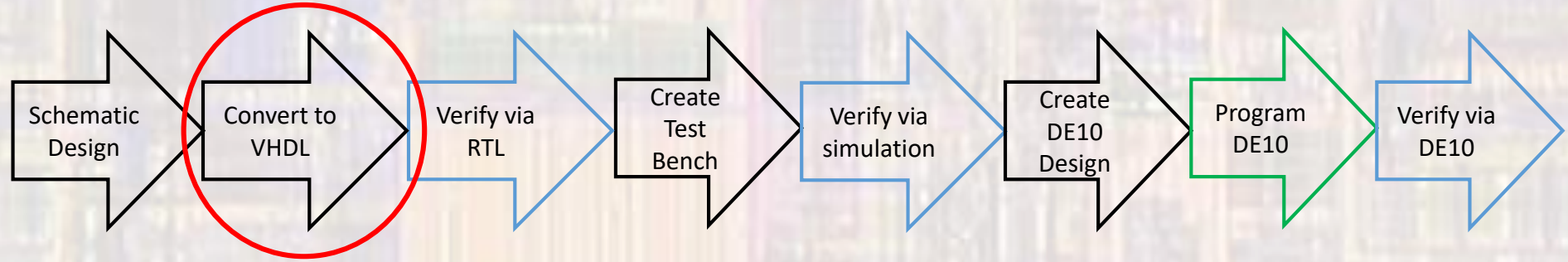
Schematic Project Example

- Create a new BDF file
  - Create your schematic



Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

myDesign_de10.vhdl

Schematic Project Example

- Create VHDL file
  - Create a VHDL file for your schematic
  - Select File → Create/Update → Create HDL Design File from Current File

```
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-- agreement, including, without limitation, that your use is for
-- the sole purpose of programming logic devices manufactured by
-- Intel and sold by Intel or its authorized distributors.  Please
-- refer to the applicable agreement for further details.

-- PROGRAM        "Quartus Prime"
-- VERSION        "Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition"
-- CREATED        "Fri Feb 23 15:52:47 2018"

LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY MyFirstLogic IS
	PORT
	(
		in_A :  IN  STD_LOGIC;
		in_B :  IN  STD_LOGIC;
		out_1 :  OUT  STD_LOGIC;
		out_2 :  OUT  STD_LOGIC
	);
END MyFirstLogic;
```

```
ARCHITECTURE bdf_type OF MyFirstLogic IS

SIGNAL  SYNTHESIZED_WIRE_12 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_13 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_14 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_4 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_8 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_9 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_10 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_11 :  STD_LOGIC;

BEGIN

SYNTHESIZED_WIRE_11 <= SYNTHESIZED_WIRE_12 AND SYNTHESIZED_WIRE_13;

SYNTHESIZED_WIRE_13 <= NOT(in_A AND in_B);

SYNTHESIZED_WIRE_4 <= NOT(in_A OR in_B);

SYNTHESIZED_WIRE_12 <= in_B AND in_A;

SYNTHESIZED_WIRE_14 <= in_A OR in_B;

SYNTHESIZED_WIRE_9 <= SYNTHESIZED_WIRE_14 OR SYNTHESIZED_WIRE_12;

SYNTHESIZED_WIRE_10 <= SYNTHESIZED_WIRE_4 AND SYNTHESIZED_WIRE_14;

SYNTHESIZED_WIRE_8 <= SYNTHESIZED_WIRE_14 AND SYNTHESIZED_WIRE_13;

out_2 <= SYNTHESIZED_WIRE_8 OR SYNTHESIZED_WIRE_9;

out_1 <= SYNTHESIZED_WIRE_10 AND SYNTHESIZED_WIRE_11;

END bdf_type;
```

Schematic Project Example

- Create VHDL file
  - Create a component template for your design (DUT)
    - Select File → Create/Update → Create VHDL Component Declaration Files from Current File

```
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-- the Intel FPGA IP License Agreement, or other applicable license
-- agreement, including, without limitation, that your use is for
-- the sole purpose of programming logic devices manufactured by
-- Intel and sold by Intel or its authorized distributors.  Please
-- refer to the applicable agreement for further details.


-- Generated by Quartus Prime Version 17.1 (Build Build 590 10/25/2017)
-- Created on Fri Feb 23 15:57:28 2018
```
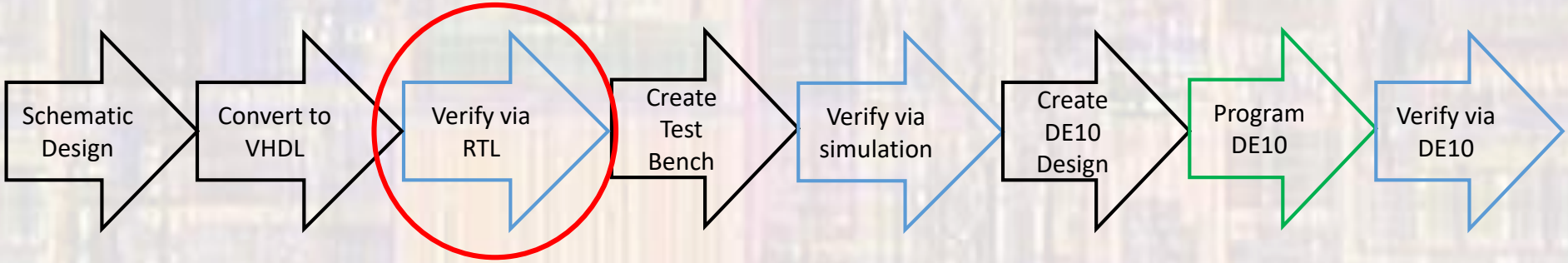

```
COMPONENT MyFirstLogic
    PORT
    (
        in_A        :    IN STD_LOGIC;
        in_B        :    IN STD_LOGIC;
        out_1       :    OUT STD_LOGIC;
        out_2       :    OUT STD_LOGIC
    );
END COMPONENT;
```

Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

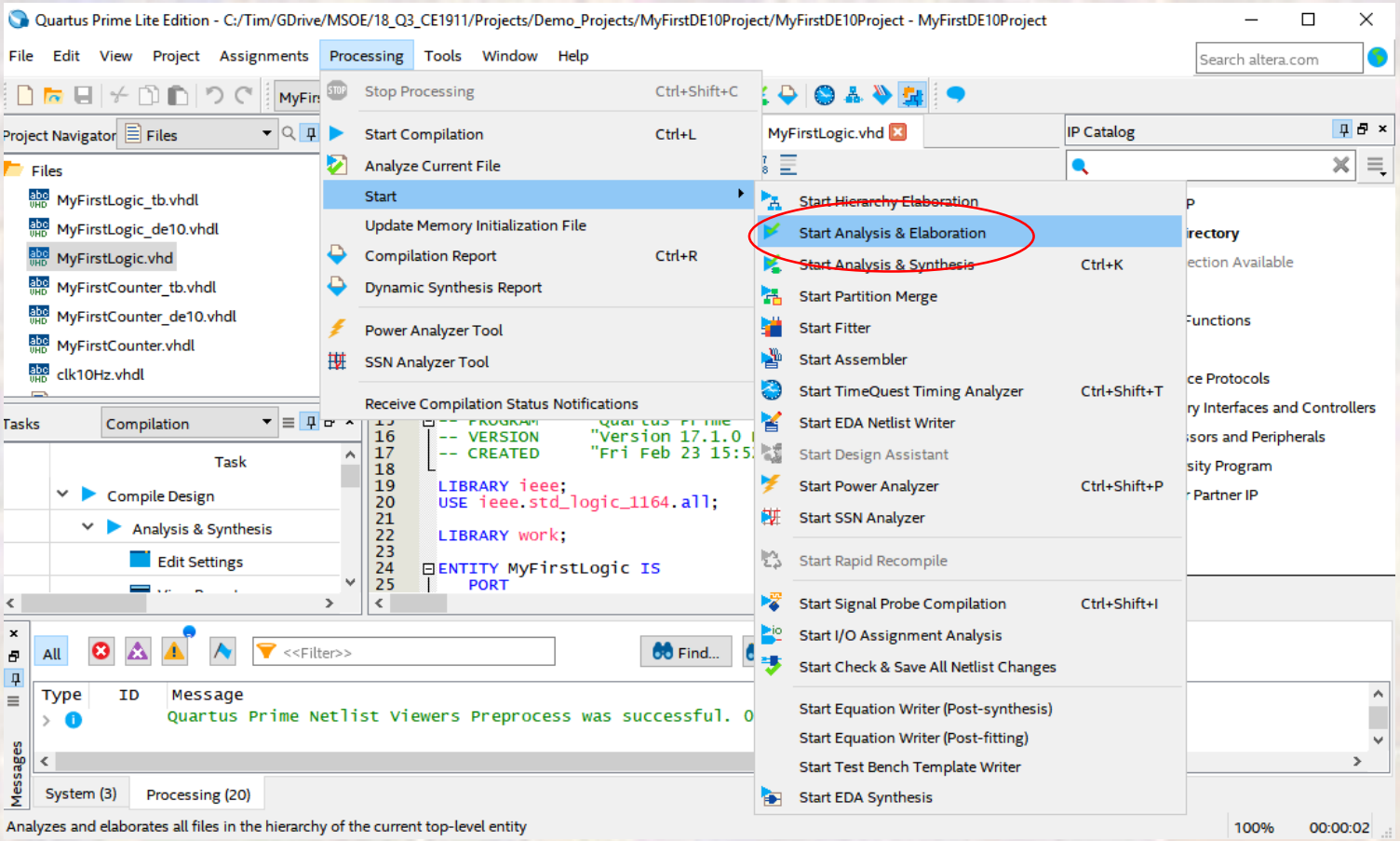
myDesign_de10.vhdl

Schematic Project Example

- Create VHDL file
  - Prepare to use the VHDL file
    - Remove the BDF file from the project
      - In project Navigator – Files, Right click the BDF file and select: Remove file from project
    - Add the created VHDL file to the project
      - Select Project → Add/remove files in project → file name …
      - Select the file to add
    - Set the VHDL file as the Top-Level Entity
      - In project Navigator – Files, Right click the VHDL file and select: Set as Top-Level Entity

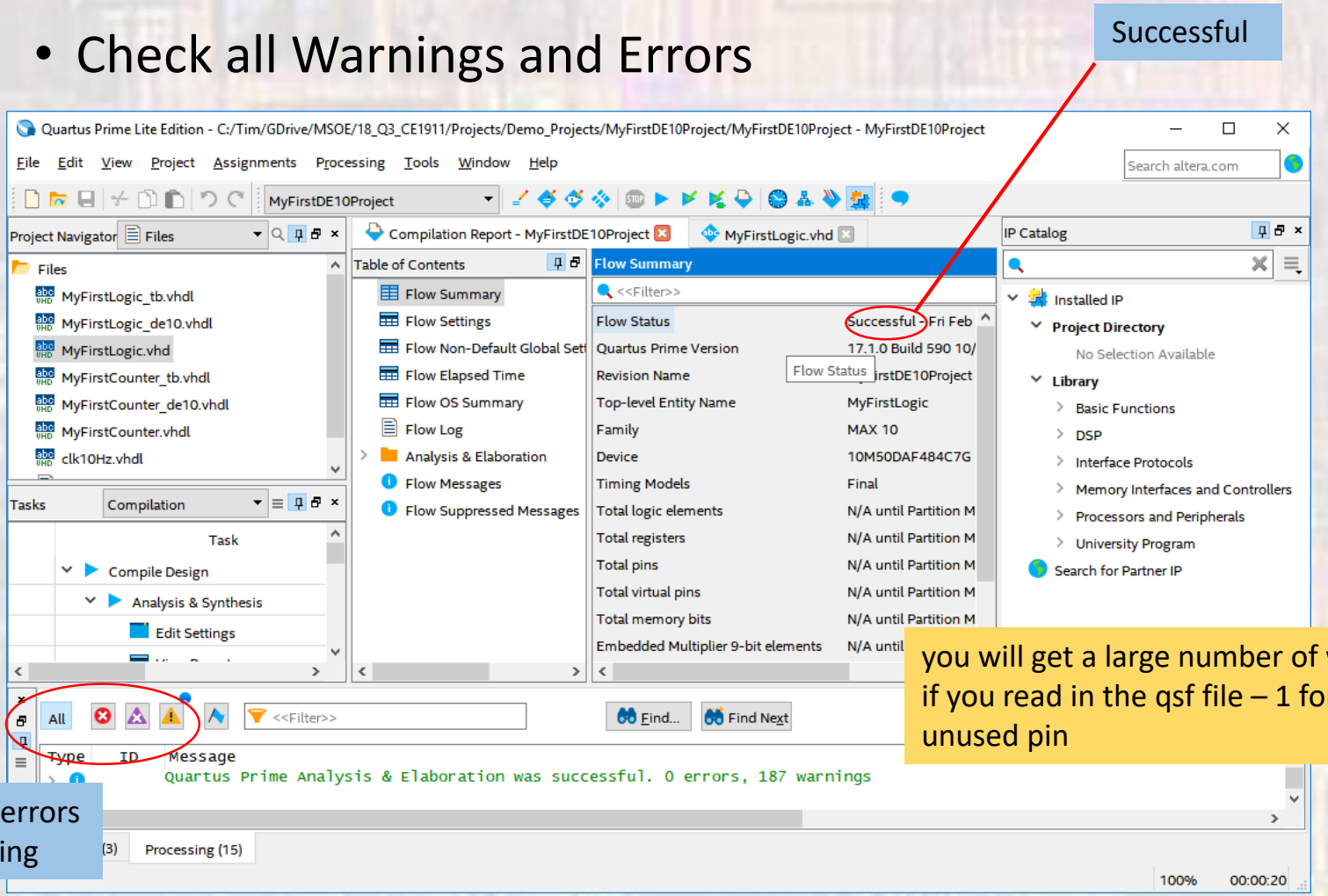
Schematic Project Example

- Create VHDL file
  - Verify your code is synthesizable
  - Select Processing -> Start -> Start Analysis & Elaboration



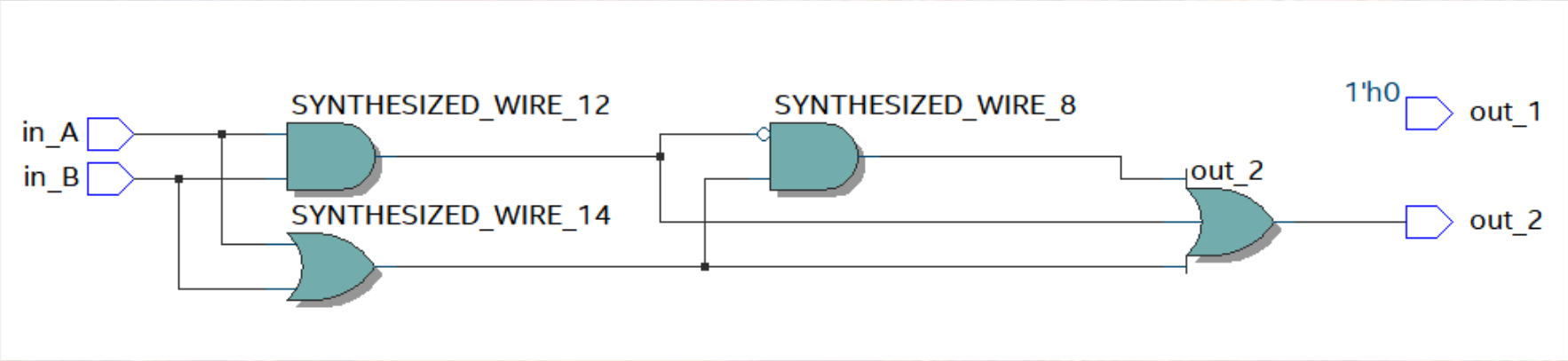
Schematic Project Example

- Create VHDL file
  - Check all Warnings and Errors



Schematic Project Example

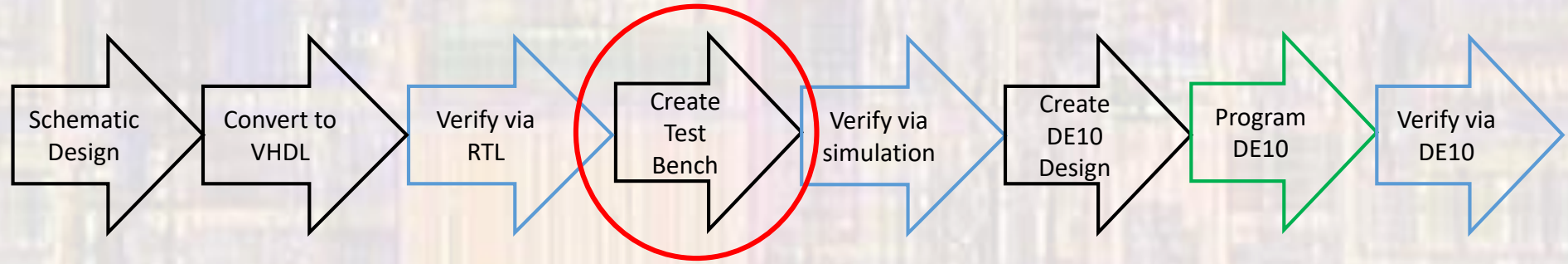
- Create VHDL file
  - ALWAYS check your RTL to make sure it makes sense
  - Select Tools → Netlist Viewers → RTL Viewer



  - Note – the new design will be optimized

Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

myDesign_de10.vhdl

Schematic Project Example

- Project Verification
  - Create a Test Bench
  - Open a new vhdl design file with the name MyFirstLogic_tb
  - Create a test bench entity and instantiate your design at the device under test (DUT)
  - Create test inputs using the non-synthesizable wait instructions

Schematic Project Example

- Project Verification
  - Create a Test Bench

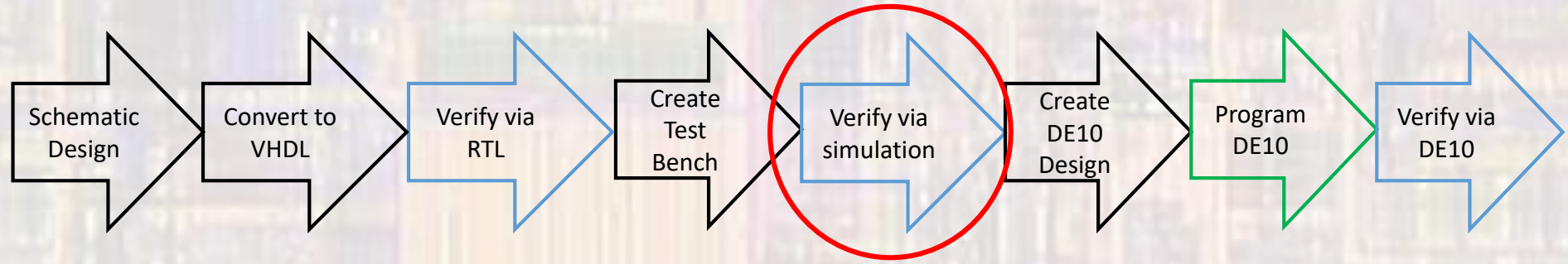
```
--------------------------------
--
-- MyFirstLogic_tb.vhdl
--
-- created: 1/26/18
-- by: johnsontimoj
-- rev: 0
--
-- testbench forlogic example
-- of MyFirstLogic.vhdl
--
-- brute force implementation
--
--------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity MyFirstLogic_tb is
   -- no entry - testbench
end entity;
```

```
architecture testbench of MyFirstLogic_tb is
   signal   IN_A:    std_logic;
   signal   IN_B:    std_logic;

   signal   OUT_1:   std_logic;
   signal   OUT_2:   std_logic;

   constant PER:  time  := 20 ns;

   ----------------------------------
   -- Component prototype
   ----------------------------------
   COMPONENT MyFirstLogic
   PORT
      (
      in_A     :   IN STD_LOGIC;
      in_B     :   IN STD_LOGIC;
      out_1    :   OUT STD_LOGIC;
      out_2    :   OUT STD_LOGIC
      );
   END COMPONENT;

   ----------------------------------
```

```
   begin

   ----------------------------------
   -- Device under test (DUT)
   ----------------------------------
   DUT: MyFirstLogic
      port map(
               in_A  => IN_A,
               in_B  => IN_B,
               out_1 => OUT_1,
               out_2 => OUT_2
               );


   ----------------------------------
   -- Brute force test process
   ----------------------------------
   brute: process    -- no sens list allowed
      begin
         ----------------------------
         -- Initialize all inputs
         IN_A <= '0';
         IN_B <= '0';
         ----------------------------
         -- run
         wait for PER;
         IN_A <= '1';
         wait for PER;
         IN_A <= '0';
         wait for PER;
         IN_B <= '1';
         wait for PER;
         IN_B <= '0';
         wait for PER;
         IN_A <= '1';
         IN_B <= '1';
         wait for PER;
         IN_A <= '0';
         IN_B <= '0';

   end process brute;
end architecture;
```

Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

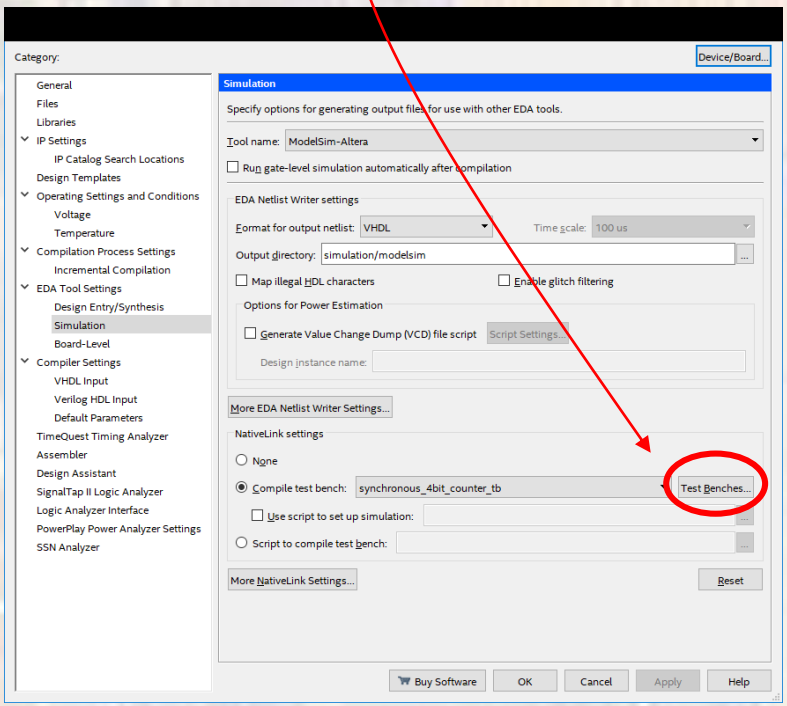
myDesign_de10.vhdl

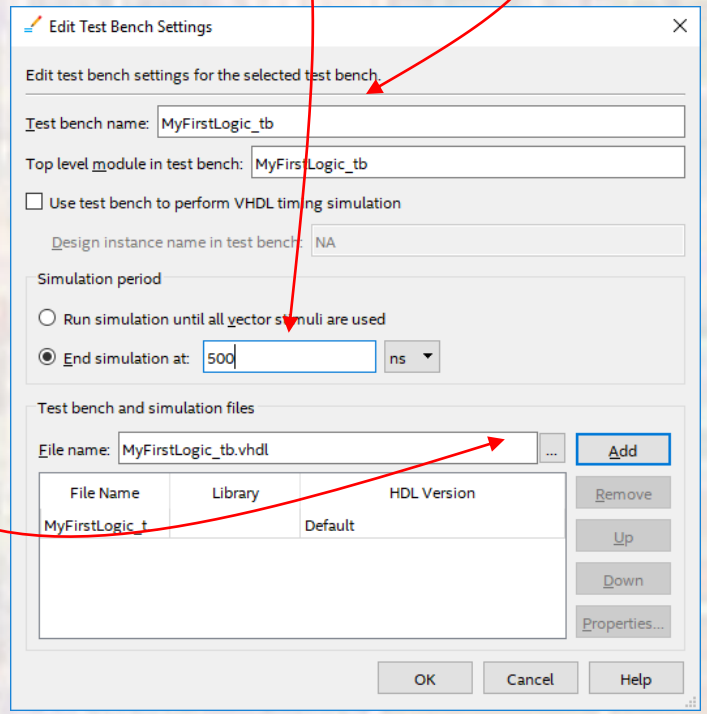
Schematic Project Example

- Project Verification
  - Elaborate the design
    - With the original vhdl design set as the top level entity (not the xxxx_tb.vhdl design)
    - Select Processing → Start → Start Analysis and Elaboration
  - This causes Quartus to check the Test Bench code along with the original vhdl design

Schematic Project Example

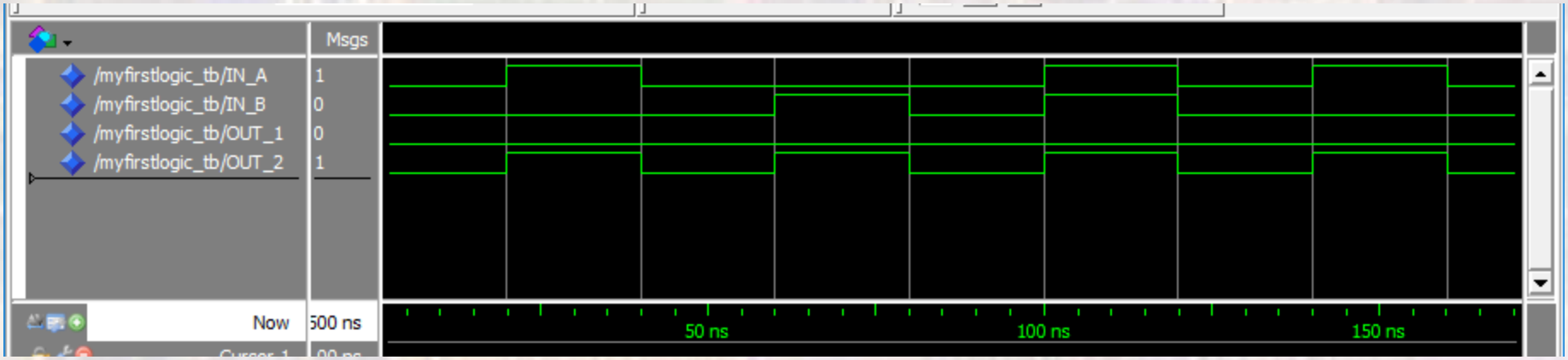
- Project Verification
  - Setup the test bench
    - Select Assignments → Settings → EDA Tool Settings → Simulation → Test Benches : enter the test bench file
      : select the end simulation time
      : select File name … and select the test bench file





Schematic Project Example

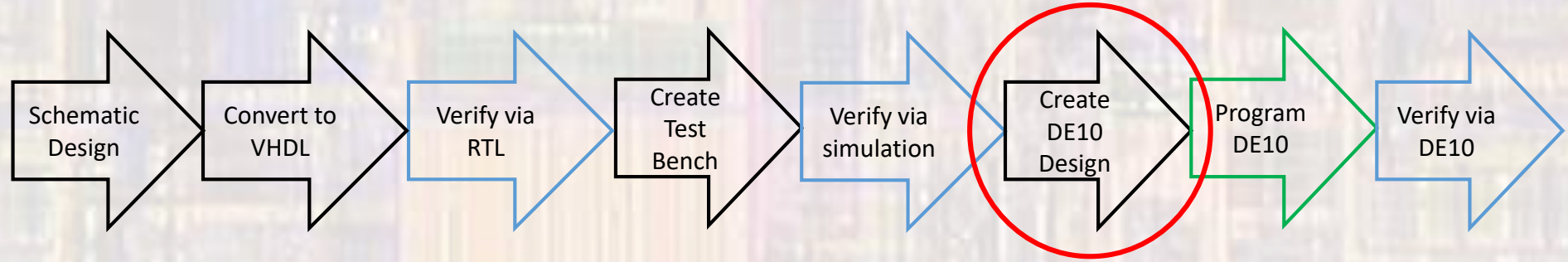
- Project Verification
  - Run the simulation
    - Select Tools → Run Simulation Tool → RTL Simulation



1 full cycle

Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

myDesign_de10.vhdl

Schematic Project Example

- Project Implementation
  - Prepare for DE10
  - Create a new VHDL File
    - MyFirstLogic_de10.vhdl
  - Use the DE10 pin names from the qsf file
    - or you can use the pin planner
  - Instantiate your Design

Schematic Project Example

- Project Implementation
  - Prepare for DE10

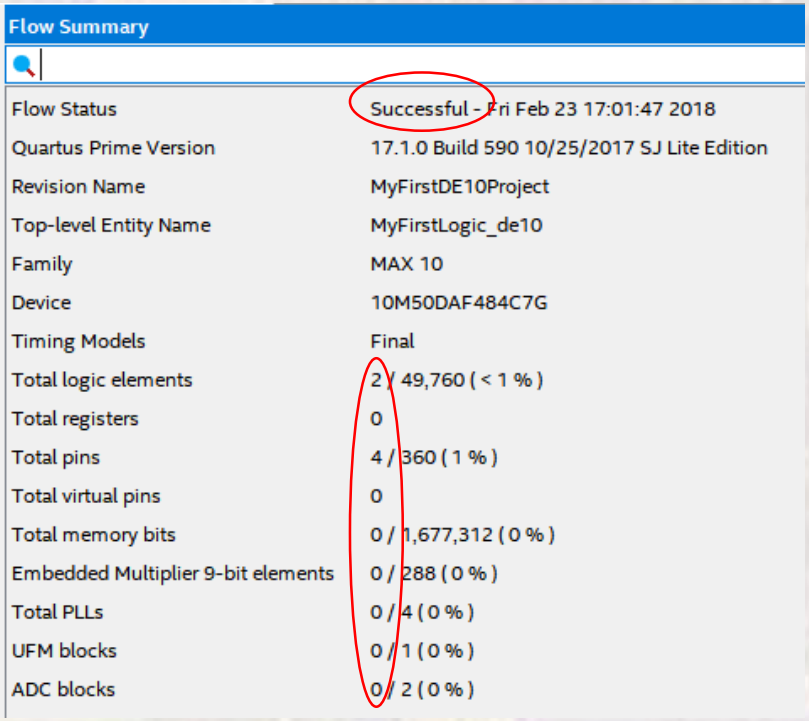
```
--------------------------------
--
-- MyFirstLogic_de10.vhdl
--
-- created: 2/23/18
-- by: johnsontimoj
-- rev: 0
--
-- DE10 file for random logic
-- of MyFirstLogic.vhdl
--
-- using qsf pin names
-- SW[0] --> in_A
-- SW[1] --> in_B
--
-- LEDR --> out_1 and out_2
--
--------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity MyFirstLogic_de10 is
   PORT(
         SW:          in std_logic_vector(1 downto 0);
         LEDR:        out std_logic_vector(1 downto 0)
         );
end entity;
```

```
architecture testbench of MyFirstLogic_de10 is


   ---------------------------------
   -- Component prototype
   ---------------------------------
   COMPONENT MyFirstLogic
   PORT
      (
      in_A      :    IN STD_LOGIC;
      in_B      :    IN STD_LOGIC;
      out_1     :    OUT STD_LOGIC;
      out_2     :    OUT STD_LOGIC
      );
   END COMPONENT;
   -----------------------------------


   begin

   -------------------------------------
   -- Design placement
   -------------------------------------
   DESIGN: MyFirstLogic
      port map(
               in_A => SW(0),
               in_B => SW(1),
               out_1 => LEDR(0),
               out_2 => LEDR(1)
               );

end architecture;
```

Schematic Project Example

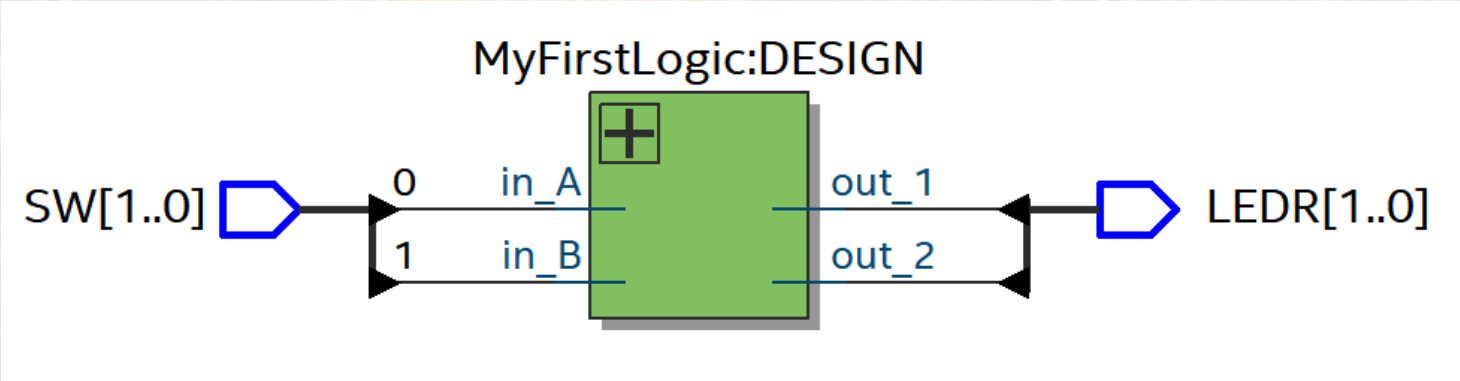
- Project Implementation
  - Prepare for DE10

  - Compile your design
  - Check the Compilation Summary



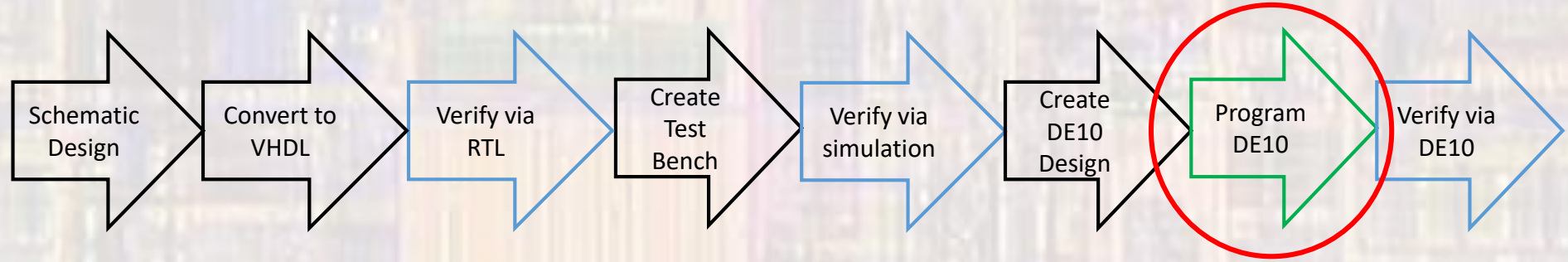
Schematic Project Example

- Project Implementation
  - Prepare for DE10
  - Check the RTL



Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

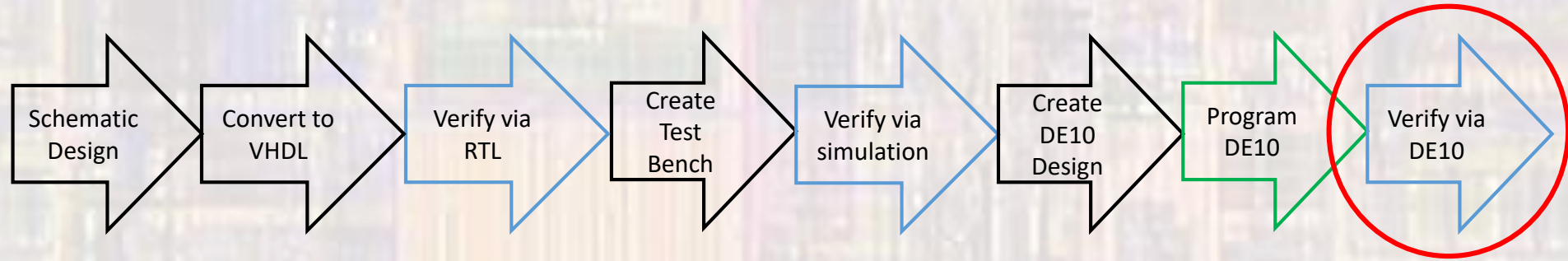
myDesign_de10.vhdl

Schematic Project Example

- Project Implementation
  - Configure the DE10
  - Select Tools -> Programmer
    - point to the compiled output file
    - start

Schematic Project Example

- Project Flow



myDesign.bdf

myDesign.vhdl

myDesign_tb.vhdl

myDesign_de10.vhdl

Schematic Project Example

- Project Implementation
  - Configure the DE10
  - Validate the design on the DE10 board