eUSCI_SPI Info Sheet

n=3:0 x=A or B

EUSCI_xn_SPI ->	CTLW0	Control Word
	BRW	Bit rate divider
	STATW	Status
	RXBUF	RX Buffer
	TXBUF	TX Buffer
	IE	Interrupt Enable
	IFG	Interrupt Flags
	IV	Interrupt Vector

EUSCIA0_IRQHandler	INTISR[16]	eUSCI_A0	UART or SPI mode TX, RX, and Status Flags
EUSCIA1_IRQHandler	INTISR[17]	eUSCI_A1	UART or SPI mode TX, RX, and Status Flags
EUSCIA2_IRQHandler	INTISR[18]	eUSCI_A2	UART or SPI mode TX, RX, and Status Flags
EUSCIA3_IRQHandler	INTISR[19]	eUSCI_A3	UART or SPI mode TX, RX, and Status Flags
EUSCIB0_IRQHandler	INTISR[20]	eUSCI_B0	SPI or I2C mode TX, RX, and Status Flags (I2C in multiple
EUSCIB1_IRQHandler	INTISR[21]	eUSCI_B1	SPI or I2C mode TX, RX, and Status Flags (I2C in multiple
EUSCIB2_IRQHandler	INTISR[22]	eUSCI_B2	SPI or I2C mode TX, RX, and Status Flags (I2C in multiple
EUSCIB3_IRQHandler	INTISR[23]	eUSCI_B3	SPI or I2C mode TX, RX, and Status Flags (I2C in multiple

PORT		PSEL[1:0]
P1.0	UC A 0 STE	01
P1.1	CLK	
P1.2	SOMI	
P1.3	SIMO	
P2.0	UC A 1 STE	01
P2.1	CLK	
P2.2	SOMI	
P2.3	SIMO	
P3.0	UC A 2 STE	01
P3.1	CLK	
P3.2	SOMI	
P3.3	SIMO	
P9.4	UC A 3 STE	01
P9.5	CLK	
P9.6	SOMI	
P9.7	SIMO	

PORT		DIR	PSEL[1:0]
P1.4	UC B 0 STE		01
P1.5	CLK		
P1.7	SOMI		
P1.6	SIMO		
P6.2	UC B 1 STE		01
P6.3	CLK		
P6.5	SOMI		
P6.4	SIMO		
P3.4	UC B 2 STE		01
P3.5	CLK		
P3.7	SOMI		
P3.6	SIMO		
P10.0	UC B 3 STE		01
P10.1	CLK		
P10.3	SOMI		
P10.2	SIMO		
P8.0	UC B 3 STE		01
P8.1	CLK		01
P6.7	SOMI		10
P6.6	SIMO		10