TIMER A Info Sheet

n=3:0 x=4:0

TIMER_An	->	CTL	Timer Control
		CCTL[x]	Capture/Compare Control
		R	Counter
		CCR[x]	Capture/Compare
		EX0	Clock Divider
		IV	Interrupt Vector

TA0_0_IRQHandler	INTISR[8]	Timer_A0	TA0CCTL0.CCIFG
TA0_N_IRQHandler	INTISR[9]	Timer_A0	TA0CCTLx.CCIFG (x = 1 through 4), TA0CTL.TAIFG
TA1_0_IRQHandler	INTISR[10]	Timer_A1	TA1CCTL0.CCIFG
TA1_N_IRQHandler	INTISR[11]	Timer_A1	TA1CCTLx.CCIFG (x = 1 through 4), TA1CTL.TAIFG
TA2_0_IRQHandler	INTISR[12]	Timer_A2	TA2CCTL0.CCIFG
TA2_N_IRQHandler	INTISR[13]	Timer_A2	TA2CCTLx.CCIFG (x = 1 through 4), TA2CTL.TAIFG
TA3_0_IRQHandler	INTISR[14]	Timer_A3	TA3CCTL0.CCIFG
TA3_N_IRQHandler	INTISR[15]	Timer_A3	TA3CCTLx.CCIFG (x = 1 through 4), TA3CTL.TAIFG

PORT				DIR	PSEL[1:0]	PORT				DIR	PSEL[1:0]
P7.3	TA0	0	CCI 0 A	0	01	P8.1	TA2	0	CCI 0 A	0	10
			Out 0 A	1	01				Out 0 A	1	10
P2.4	TA0	1	CCI 1 A	0	01	P5.6	TA2	1	CCI 1 A	0	01
			Out 1 A	1	01				Out 1 A	1	01
P2.5	TA0	2	CCI 2 A	0	01	P5.7	TA2	2	CCI 2 A	0	01
			Out 2 A	1	01				Out 2 A	1	01
P2.6	TA0	3	CCI 3 A	0	01	P6.6	TA2	3	CCI 3 A	0	01
			Out 3 A	1	01				Out 3 A	1	01
P2.7	TA0	4	CCI 4 A	0	01	P6.7	TA2	4	CCI 4 A	0	01
			Out 4 A	1	01				Out 4 A	1	01
P7.1	TA0		CLK	0	01	P4.2	TA2		CLK	0	10
P8.0	TA1	0	CCI 0 A	0	10	P10.4	TA3	0	CCI 0 A	0	01
			Out 0 A	1	10				Out 0 A	1	01
P7.7	TA1	1	CCI 1 A	0	01	P10.5	TA3	1	CCI 1 A	0	01
			Out 1 A	1	01				Out 1 A	1	01
P7.6	TA1	2	CCI 2 A	0	01	P8.2	TA3	2	CCI 2 A	0	01
			Out 2 A	1	01				Out 2 A	1	01
P7.5	TA1	3	CCI 3 A	0	01	P9.2	TA3	3	CCI 3 A	0	01
			Out 3 A	1	01				Out 3 A	1	01
P7.4	TA1	4	CCI 4 A	0	01	P9.3	TA3	4	CCI 4 A	0	01
			Out 4 A	1	01				Out 4 A	1	01
P7.2	TA1		CLK	0	01	P8.3	TA3		CLK	0	01