VHDL Basics

- VHDL – Selection
  - if-else
    - Choose a value when a certain situation exists

```
if (decision_signal = decision_value_X) then
  result_signal_1 <= result_value_1;
  result_signal_2 <= result_value_2;
  result_signal_3 <= result_value_3;
elsif (decision_signal = decision_value_Y) then
  result_signal_1 <= result_value_1a;
  result_signal_2 <= result_value_2b;
  result_signal_3 <= result_value_3c;
else
  result_signal_1 <= result_value_a;
  result_signal_2 <= result_value_b;
  result_signal_3 <= result_value_c;
end if;
```

Typically use the same decision signal
Exception – creating registers (Flip-Flops)

Limitation: Must be used in a process

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Exhaustive List

```
if(inA = "00") then
   outW <= "1000";
elsif(inA = "01") then
   outW <= "0100";
elsif(inA = "10") then
   outW <= "0010";
elsif(inA = "11") then
   outW <= "0011";
else
   outW <= "0000";
end if;
```

Partial List

```
if(inA = "00") then
   outX <= "1000";
elsif(inA = "01") then
   outX <= "0100";
else
   outX <= "0000";
end if;
```

Partially Common Result

```
if(inA = "00") then
   outY <= "1000";
elsif(inA = "01") then
   outY <= "0100";
elsif((inA = "10") or (inA = "11")) then
   outY <= "0110";
else
   outX <= "0000";
end if;
```

Complex Selection

```
if((inA or inB) = "00") then
   outZ <= "1000";
elsif((inA or inB)  = "01") then
   outZ <= "0100";
else
   outZ <= "0000";
end if;
```

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- VHDL – Selection
  - if-else

```
----------------------------------------
--
-- if_else.vhdl
--
-- created 7/5/2018
-- tj
--
-- rev 0
----------------------------------------
--
-- if-else example
--
----------------------------------------
--
-- Inputs: inA, inB, inC
-- Outputs: outV, outW, outX, outY, outZ
--
----------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity if_else is
    port (
        inC:    in std_logic_vector(3 downto 0);
        outV:   out std_logic_vector(3 downto 0)
);
end entity;
```

```
architecture behavioral of if_else is

begin
    process(all)
    begin
        if(inC = "0000") then
            outV <= "0001";
        elsif(inC = "0001") then
            outV <= "0010";
        elsif(inC = "0010") then
            outV <= "0011";
        elsif(inC = "0011") then
            outV <= "0100";
        elsif(inC = "0100") then
            outV <= "0101";
        elsif(inC = "0101") then
            outV <= "0110";
        elsif(inC = "0110") then
            outV <= "0111";
        elsif(inC = "0111") then
            outV <= "1000";
        elsif(inC = "1000") then
            outV <= "1001";
        else
            outV <= "0000";
        end if;
    end process;
end behavioral;
```

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