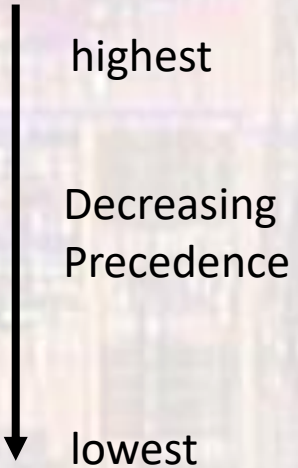
# VHDL Operator Precedence

- Operator Groups

| | | | | | | |
|---|---|---|---|---|---|---|
| Misc: | ** | abs | not | | | |
| Multiplying: | * | / | mod | rem | | |
| Sign: | + | - | | | | |
| Adding: | + | - | & | | | |
| Shift: | sll | srl | sla | sra | rol | ror |
| Relational: | = | /= | < | <= | > | >= |
| Logical: | and | or | nand | nor | xor | xnor |




- There is no precedence defined within a group – must use parenthesis to define order

```
B <= A or C and D     -- Illegal
B <= (A or C) and D   -- legal
```

- Best practice is to use parenthesis in all cases