Comparator Pinout

- Comparator Connections - Inputs
  - Nucleo-L476RG uses programmable I/O selection to choose the INP and INM connections
  - Multiple steps are required to enable these connections
    - Port(s) must be enabled (clocks enabled)
    - Pins must be selected as Analog Inputs (using the Pin I/O configuration registers)
    - Pins must be selected in the COMPx registers

Table 143. COMP1 input plus assignment

COMP1_INP	COMP1_INPSEL
PC5	0
PB2	1

Table 144. COMP1 input minus assignment

COMP1_INM	COMP1_INMSEL[2:0]
¼ V_{REFINT}	000
½ V_{REFINT}	001
¾ V_{REFINT}	010
V_{REFINT}	011
DAC Channel1	100
DAC Channel2	101
PB1	110
PC4	111

Table 145. COMP2 input plus assignment

COMP2_INP	COMP2_INPSEL
PB4	0
PB6	1

Table 146. COMP2 input minus assignment

COMP2_INM	COMP2_INMSEL[2:0]
¼ V_{REFINT}	000
½ V_{REFINT}	001
¾ V_{REFINT}	010
V_{REFINT}	011
DAC Channel1	100
DAC Channel2	101
PB3	110
PB7	111

Comparator Pinout

- Comparator Connections - outputs
  - Nucleo-L476RG uses programmable I/O selection for the OUT connection
  - Multiple steps are required to enable these connections
    - Port must be enabled (clocks enabled)
    - Pins must be configured to allow Alternate Function
    - The COMPx output must be selected as the alternate function

Table 18. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_BK1_IO1	LCD_SEG5	COMP1_OUT	-	-	EVENTOUT
	PB1	-	-	QUADSPI_BK1_IO0	LCD_SEG6		-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	-	-	LCD_SEG7	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_DE	TSC_G2_IO1	-	LCD_SEG8	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2_COMP2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	-	LCD_SEG21	FMC_NL	TIM8_BKIN_COMP1	TIM17_CH1N	EVENTOUT
	PB8	-	CAN1_RX	-	LCD_SEG16	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-	LCD_COM3	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_NCS	LCD_SEG11	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS_DE	TSC_G1_IO1	-	LCD_SEG12	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	-	LCD_SEG13	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	LCD_SEG14	SWPMI1_RX	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	LCD_SEG15	SWPMI1_SUSPEND	SAI2_SD_A	TIM15_CH2	EVENTOUT